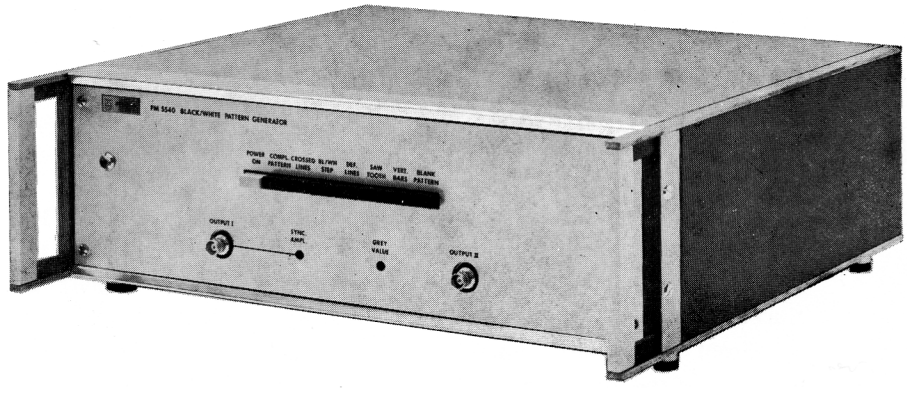
Black/White
Pattern Generator
PM 5540

9449 055 40...1

9499 490 04311

1/971/2/02-08

PHILIPS



operating and service manual

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In correspondence concerning this instrument, please quote the complete type and serial number, as given on the identification plate at the rear of the instrument.

1 Introduction

The PHILIPS PM 5540 is an extremely stable professional source of electronic test patterns.
It has been designed for use when developing and manufacturing television receivers, in television laboratories, in television studios and in television broadcasting stations.
The synchronizing and blanking signals are obtained from a PHILIPS TV-pulse generator PM 5530.

II Technical data

Properties expressed in numerical values with tolerances stated, are guaranteed by us. Numerical values without tolerances stated, represent the properties of an average instrument and merely serve as a guide.

A PM 5540E (CCIR-version) can be converted to a PM 5540A (RTMA-version) by modifying four units (memory, line decoder, line register and vertical divider).

1. Inputs

Sync. and blanking	Amplitude: 2-8 V_{pp} negative
External video	Amplitude: 0.7 V_{pp}, exclusive sync. External synchronized video information is added linearly to the signal present on "OUTPUT I".
Input impedance	High

2. Outputs

Video output I	Nominal output 1 V_{pp} inclusive sync. Sync. ampl. is adjustable approx. 0-200 % by screwdriver control on front panel ("SYNC.AMPL.") Video signal (excl.sync.) can internally be adjusted from 0.5 V_{pp} to 1 V_{pp}.
Video output II	Amplitude 1 V_{pp}, inclusive sync.
Output impedance	75 Ω
Set-up	no set-up; can be added (see checking and adjusting unit 16).

3. Rise time-pulse width etc.

Rise and decay time of video transitions	< 100 nsec.
Pulse width of vertical lines and needle pulse	200 nsec. ± 20 nsec. (T 50 %)
Width of horizontal lines	2 picture lines, one in each field.
Definition lines	Square waves having frequencies of 0.8-1.8-2.8-3.8-4.8 MHz ± 2 %, fixed phase relation. Rise time approx. 50 ns.

4. Linearity

Grey scale staircase	5 equal steps, amplitude of each step within ± 10 % of each nominal value.
Line sawtooth	Direction black-white, full video amplitude.

5. Power supply

Voltage	115/230 V ± 20 % to be selected by a 2 position switch.

Mains frequency	50-60 Hz
Consumption	40 W at 220 V.
Fuse	For 90-160 V: 500 mA, delayed action For 180-320 V: 250 mA, delayed action

6. Temperature range

Operating conditions –10° to +45° C.

7. Mechanical specification

Width: 19".
Height: 3 units = 150 mm, incl. feet
Depth: 420 mm, including handles.
Weight: 11.5 kg.
The instrument is delivered as a table model, but can be easily converted into a 19" rack model.

8. Versions

PM 5540A	for RTMA – 525 lines system
PM 5540E	for CCIR – 625 lines system

III Accessories

With the instrument are delivered
1 operating- and service manual
1 mains cable
7 BNC connectors
5 BNC connectors with 75Ω load.

IV Description of simplified block diagram

1. Input amplifier
The instrument has to be driven with 2 signals ("SYNC"-"BLANKING"), available from e.g. a PHILIPS TV pulse-generator PM 5530. It has a high input impedance and contains circuits which make the performance independent of the amplitude of the input pulses.

2. Vertical divider and decoder
This section generates all the gating signals on a field frequency basis. The signals are decoded to give the horizontal lines as well as the intervals in vertical direction.

3. Horizontal divider and decoder
The line gating signals are derived from an oscillator, controlled by the line pulses. The signals are decoded to give the gating pulses in the horizontal direction.

4. Circle generator
The circuitry used is based on digital techniques. The gating signals are obtained from a counting register, being operated from a clock-frequency oscillator.
The register is set for each line from a non-destructive ferrite-core-memory. The information is read-out from the memory line after line, selected by the line register. The electronic circle is completely locked to the rest of the pattern.

5. Cross-bar generator
This section generates the grey background, the horizontal and vertical white lines as well as the black-white squares at the borders.

6. Gradation
The 5 gradation steps are obtained by adding together suitable output signals of the horizontal divider.

7. Saw-tooth information
The saw tooth is made by charging a capacitor with a constant current generator.

8. Black-white steps and vertical bars
These signals are obtained by adding together suitable output signals of the horizontal divider.

9. Definition lines
The definition lines are generated by a square-wave oscillator controlled by a vertical or a horizontal step signal.

10. Adder circuit
The signals from the pattern generators are added together in a resistive matrix.

11. Output amplifier
The two amplifiers have 75 Ω output impedance and supply the complete video signal including sync.
Furthermore through one of the amplifiers a synchronized external video signal can be added to the electronic test-pattern.

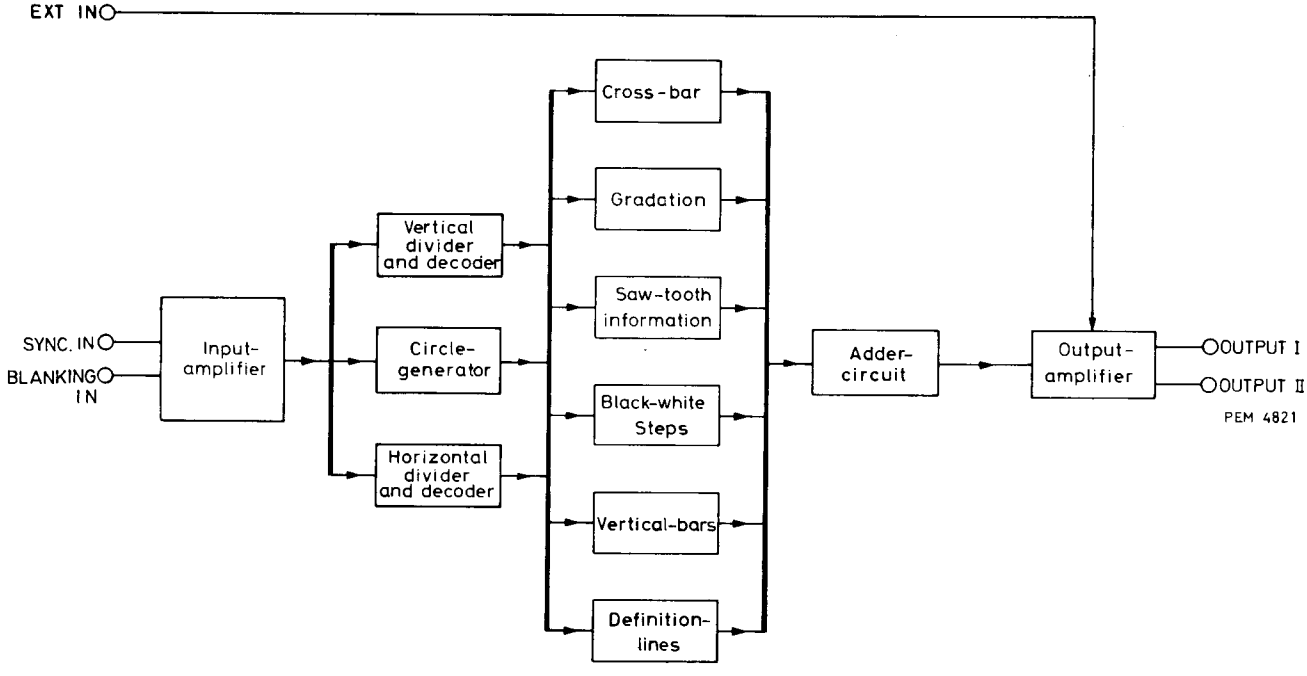


Fig. IV-1 Simplified block-diagram

V Installation

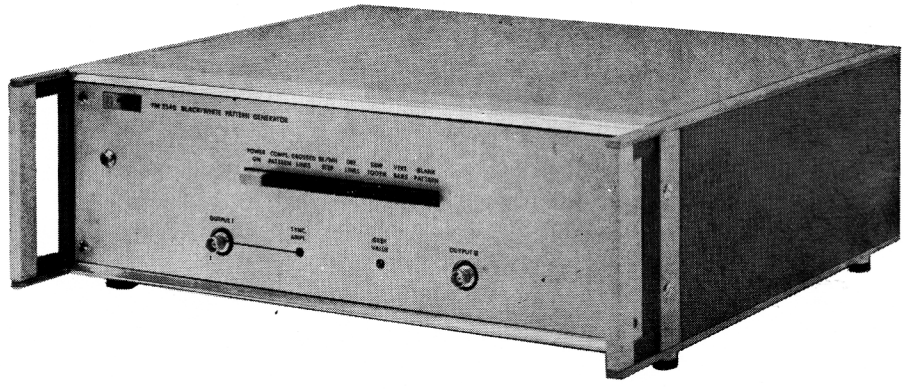


Fig. V-1 Front view of the instrument

A. Adjusting to the local mains voltage

By means of the voltage selector SK9 the instrument can be adjusted to mains voltages of 115 V or 230 V, ± 20 % (50-60 Hz).
The selected value can be read near the switch.

The instrument can be adjusted to the other mains voltage as follows:

- loosen screw "A" (Fig. V-2):
- set the switch to the desired voltage range:
- fasten screw "A" again:
- replace fuse VL1:
  for 115 V – 500 mA (delayed-action type)
  for 230 V – 250 mA (delayed-action type)

B. Earthing

Earth the instrument in accordance with the local safety regulations.

The metal cabinet can be earthed via:

socket BU12 (see Fig. V-2) and the earthing core of the mains lead.

The electrical circuit can be earthed via:

socket BU11 (see Fig. V-2) and the screening of the coaxial connection cables.

Avoid double earthing of the electrical circuit, because this may introduce hum phenomena.

C. Mounting in a 19" rack

- Remove the four screws "B" (Fig. V-2).
- Remove the four feet "C" (Fig. V-2) by turning them anti-clockwise.
- Screw the feet into the threaded holes (of screws "B") in the rear-panel.

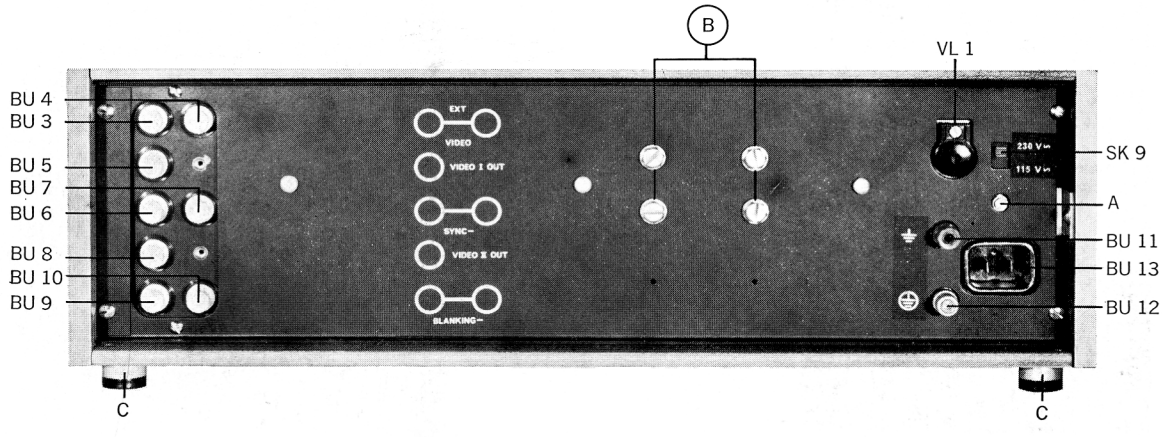


Fig. V-2 Rear view of the instrument

- Remove the screws "D" (Fig. V-3) and pull the brackets "E" out.
- Insert the bracket "E" as shown in Fig. V-4.
- The instrument can now be mounted in a 19" rack with screws inserted through the holes "F" in the brackets.

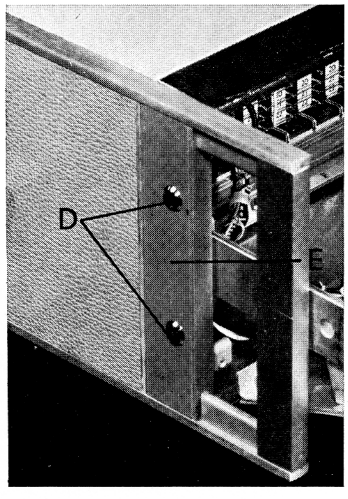


Fig. V-3 Side view

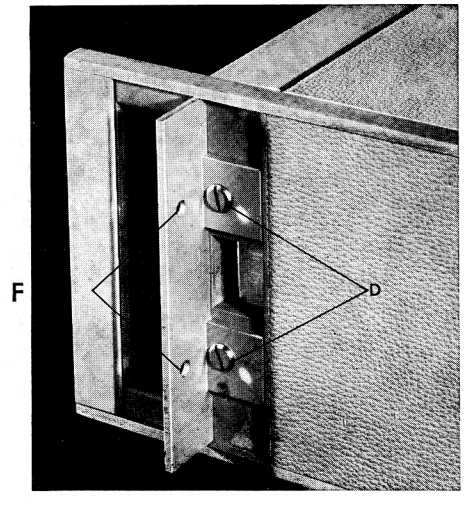


Fig. V-4 Side view

VI Survey of controls and sockets

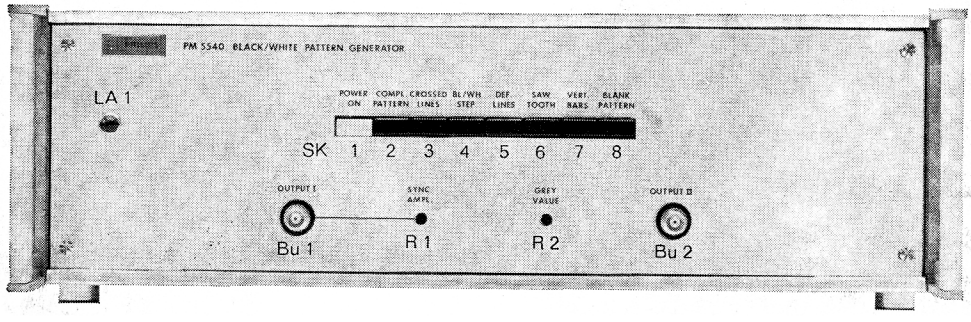


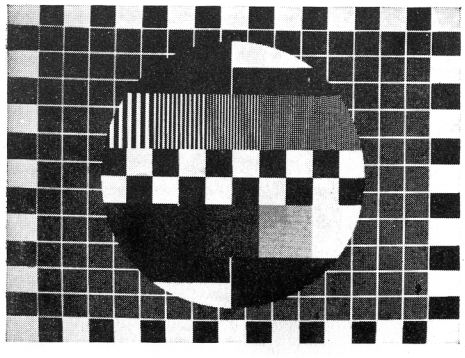
Fig. VI-1 Front view of the instrument

A. Front of the instrument

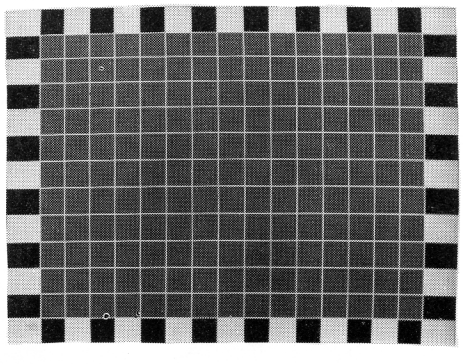
Test patterns at "VIDEO I OUT" and "VIDEO II OUT" by depressing push-button:

SK1 "POWER ON"
Mains switch

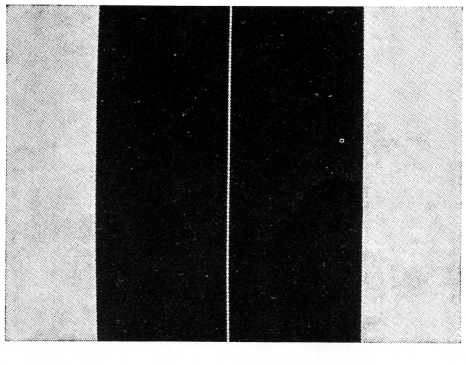
SK2 "COMPL. PATTERN"



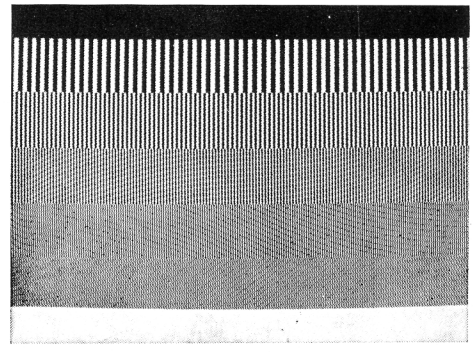
SK3 "CROSSED LINES"



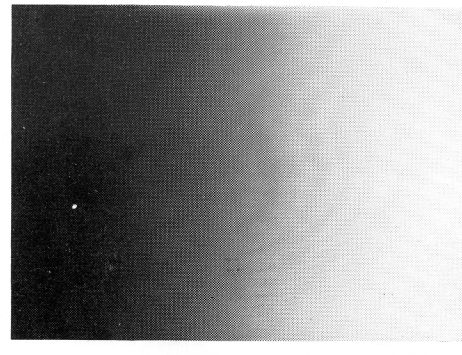
SK4 "BL/WH STEP"



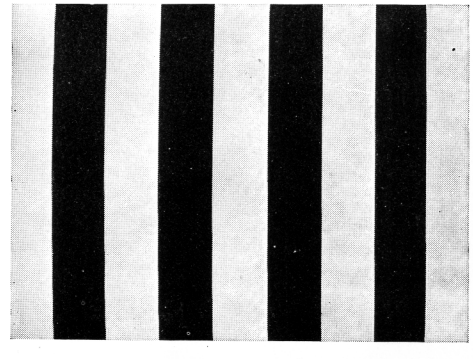
SK5 "DEF. LINES"



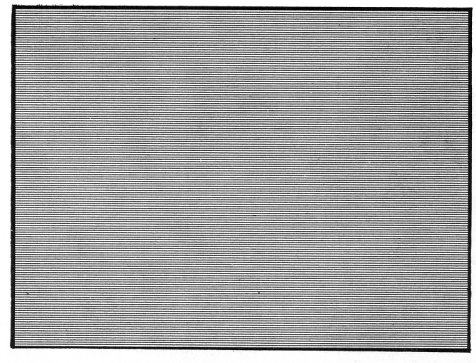
SK6 "SAW TOOTH"



SK7 "VERT. BARS"



SK8 "BLANK PATTERN"



R1 "SYNC. AMPL."
For varying the amplitude of the sync. pulses of the pattern at "OUTPUT I" between 0 and 200 %

R2 "GREY VALUE"
To vary the grey value of the "BLANK PATTERN"-signal

BU1 "OUTPUT I"
Output socket for the selected test pattern.
Amplitude: 1 V_{p-p} inclusive sync.
Sync. ampl. adjustable 0-200 % (see description of R1)

B. Rear of the instrument

BU3 and BU4 "EXT. VIDEO"
Input socket for a synchronized external video signal; This signal will be added linearly to the internal signal on BU1 "OUTPUT I".
Amplitude: 0.7 V_{p-p} (excl. sync.)
Polarity: White positive-sync. negative
Input impedance: High (The signal can be looped through)

BU5 "VIDEO I OUT"
Output socket for the selected test pattern
Interconnected with BU1 "OUTPUT I" (front)

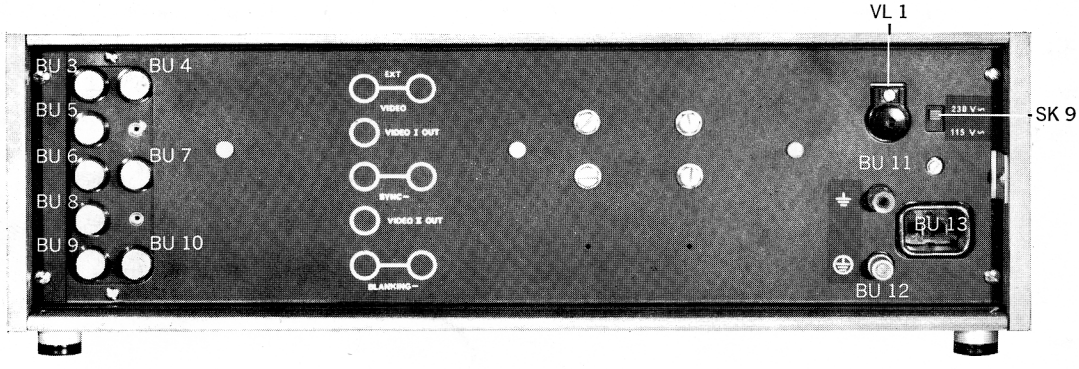


Fig. VI-2 Rear view of the instrument

Vision ampl. internally adjustable 0.7-1.4 V_{p-p}.
Polarity: White positive-sync. negative
Output impedance: 75Ω
Interconnected with BU5: "VIDEO I OUT" (rear)
(See also description of BU3: "EXT. VIDEO")

BU2 "OUTPUT II"
Output socket for the selected test pattern
Amplitude: 1 V_{p-p} inclusive sync.
Polarity: White positive – sync. negative
Output impedance: 75 Ω
Interconnected with BU8: "VIDEO II OUT" (rear)
Separated from BU1: "OUTPUT I".

BU6 and BU7 "SYNC."

Input socket for the complete synchronizing signal	Amplitude: 2-8 V_{p-p} Polarity: negative Input-impedance: high

BU8 "VIDEO II OUT"
Output socket for the selected test pattern
Interconnected with BU2 "OUTPUT II" (front)

BU9 and BU10 "BLANKING"

Input socket for the blanking signals	Amplitude: 2-8 V_{p-p} Polarity: negative Input-impedance: high

BU11 "⏚"
Earth terminal: connected to the common of the circuits of the instrument

BU12 "⏚"
Earth terminal: connected to the cabinet of the instrument

BU13
Mains socket

Sk9 "115 V~ – 230 V~"
Mains voltage selector

VL1
Fuse for 115 V mains, 500 mA, delayd-action
for 230 V mains, 250 mA, delayd-action

C. Changing testpatterns

To fulfil special demands of users, the display of some testpatterns can be altered slightly.

However, one should bear in mind that return to the original situation is not easy because the alternations are made by modifying some of the internal circuits.

a. Removing the black/white squares, surrounding the test patterns "COMPL. PATTERN" AND "CROSSED LINES".
From Unit 15 ("CROSSBAR GATE") remove diodes GR2-3-4-5-15-16-17-23-24-27 and 30.

b. Removing the lowest needle pulse (inside the circle) from test pattern "COMPL. PATTERN".
From Unit 13 ("BLACK/WHITE STEPS") remove diodes GR20 and 21.

D. Connections

Apply the following signals to the indicated sockets at the rear:
– Complete sync. signal to socket "SYNC.-"
– Complete blanking signal to socket "BLANKING-"
These signals can be taken from the PHILIPS TV-pulse generator PM 5530.
If desired, connect a synchronized video signal to "EXT. VIDEO"

NOTE:
When sockets BU4, BU7 and BU10 are not used for linking-through purposes, they should be terminated with the supplied 75 Ω-loads. Sockets "VIDEO I OUT" and "VIDEO II OUT" on the rear are connected in parallel to sockets "OUTPUT I" and "OUTPUT II" resp. on the front. The output impedance is already 75 Ω, so they should not be terminated when they are not used.

VII The principle of the circle generator

The circle on the TV screen is built up of a number of line-segments BCD (Fig. VII-1). For each line of the pattern the length of BCD has a very definite value, determined by the size of the circle.
The size of the circle in proportion to the entire TV pattern is expressed in quantities of time, (the time it takes to scan the line segments AB, BD respectively). This time has been converted into a binary figure that is characteristic for each single line. The conversion of the binary figure into time is made in an electronic counter or register, which counts a number of pulses from a clock-pulse oscillator. For each line the circle register counts the number of pulses corresponding to the distance AB.

In this way the semicircle B is converted into a number of figures, each line having its typical binary figure, corresponding to the distance AB.
These figures are stored in a magnetic-core memory from which they are transferred to the circle register for each line. The right semicircle D is made as an image of the left semicircle, as BC = CD.
In each field the circle will contain 220 lines.
The lengths of the line-segments AB, BC and CD correspond to a whole number of clock-pulses, the frequency of which (approx. 17 MHz) is high enough to produce a sufficiently smooth circle. At a lower frequency the circle would be serrated.

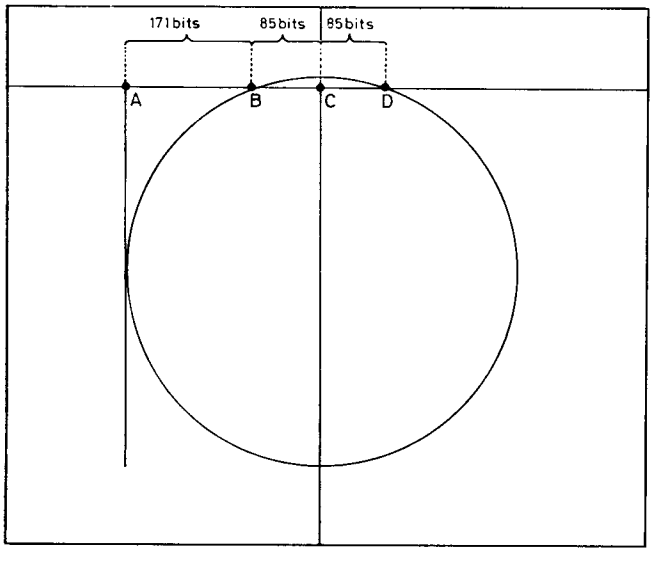


Fig. VII-1 Principle of the circle generator

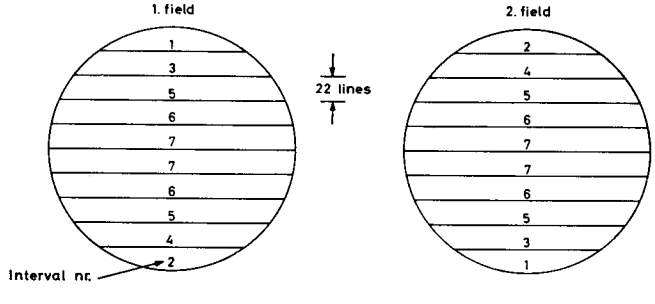


Fig. VII-2 Intervals of the two fields

The time it takes to scan the line ABC will be 15 μs., while the number of clock pulses (bits) covering this time should be a "round" binary figure, i.e. 2, 4, 8, 16, 32, 64, 128, 256 or 512.
In practice 256 bits will meet the requirements, which results in a frequency of approx. 17 MHz.

$$\left(\begin{array}{c} 256 \\ 15000 \text{ ns} \end{array} \right)$$

A. The Circle register

The memory contains information about the distance AB for each line. This information is stored in binary form.
Fig. VII-1 shows, for example, a line, for which the distance AB is equal to 171 clock pulses (bits), and the distance BC to 256 – 171 = 85 bits.
The figure 171 is in binary form = 10101011, and at the beginning of the line in question, this figure is read out of the memory and put into the circle register, which will thus be set for this figure.
At point A the 17 MHz oscillator is started, and the register begins to count. The register is connected so that it counts down from the set figure 10101011 to zero.
Passing zero the register delivers a pulse to the flip-flop oscillator which determines point B on the circle; thereby the distance AB will correspond exactly to 171 pulses The register continues counting, until the centre line of the circle is reached (in this example it has counted 85 bits). At the centre line C an external pulse is supplied to the register, which makes it change over to counting in the opposite direction.
After having counted again 85 pulses, zero is reached once more, and a pulse triggers again the flip-flop oscillator, which determines the point D on the circle. Therefore the distance CD will be the same as the distance BC on the circle.

B. The Memory

The amount of information to be stored in the memory is so large that a ferrite core is the obvious solution.
For each line the counter of the circle register is actuated, so that it forms the correct binary figure. For a circle with 220 lines it should be done by means of a rectangular matrix with 220 inputs and 8 outputs, this means a matrix with 8 × 220 = 1760 cores.
However, the size of the memory has been reduced considerably by dividing the circle in groups of lines (intervals), each containing 22 lines, as will be described later on. The size of the memory will, therefore, only be 22 × 8 = 176 cores.
The one wanted of a 22 line-group is selected during the read-out time, and the read-in is effected by means of different read-in wires, one for each interval. So the real memory function has been placed in the wiring of the read-in wires. Each wire passes some cores, and bypasses others, depending on the value of the binary figure. Consequently, the threading of the interval wires through the cores is rather complicated.
As soon as the interval wires have distributed the information over the 22 binary figures as magnetism in the cores selected, the figures are read-out line after line.
When the read-out of the 22nd line is finished, the interval wires for the next interval will place another 22 binary figures in the memory, and then these figures are read-out and transferred to the register, etc.

C. Line-selector register

As mentioned, the memory is sensed line after line through the successive 22 lines. For this process 22 sensing wires and 22 continuous sensing pulses would be necessary. The 22 pulses could be obtained from a shift register of 22 positions and triggered by line pulses.
Instead of this a binary divider (line-selector register) is used, followed by a decoder unit (line-selector decoder). Each binary figure will be decoded and delivers control signals for each single line.
This simplification of the "decoder matrix" is made by placing part of the decoding in the threading of the memory. Instead of decoding down to 22 pulses, the decoder delivers 4 × 6 pairs of pulses on only 10 sensing wires. (X- and Y-wires). Each sensing line actually consists of 2 wires connected in parallel. Only when the pulses of the two wires are in phase, the current will be strong enough to magnetize the cores and to produce an output signal for the counting register. Out of 24 (4 × 6) combination for the CCIR system only 22 will be used. For the RTMA system 20 are used and for the French system all 24.

D. Interval selector

The circle is built up of 220 lines in each field, and these lines are divided into 10 groups of intervals, each containing 22 lines. For a complete frame of two consecutive fields 20 intervals will be needed in total. However, not all intervals are different. The interlacing, which in principe makes the two fields different, has no influence on the central part of the circle, so the 6 intervals, numbered 5, 6, 7 in Fig. VII-2, in the middle of the circle can be used for both fields. The two intervals at the top of the first field can be considered an image of the corresponding intervals at the bottom of the second field. Consequently, only 4 intervals are needed for this part of the circle, and the whole circle can be built up of 4 + 3 = 7 intervals. The placing of these intervals in the circle is shown in Fig. VII-2. To select the right interval for the right place in the circle, the interval selector is used. It consists of a number of gates and is supplied with pulses, which, according to certain combinations, will deliver magnetizing forces in the correct succession.

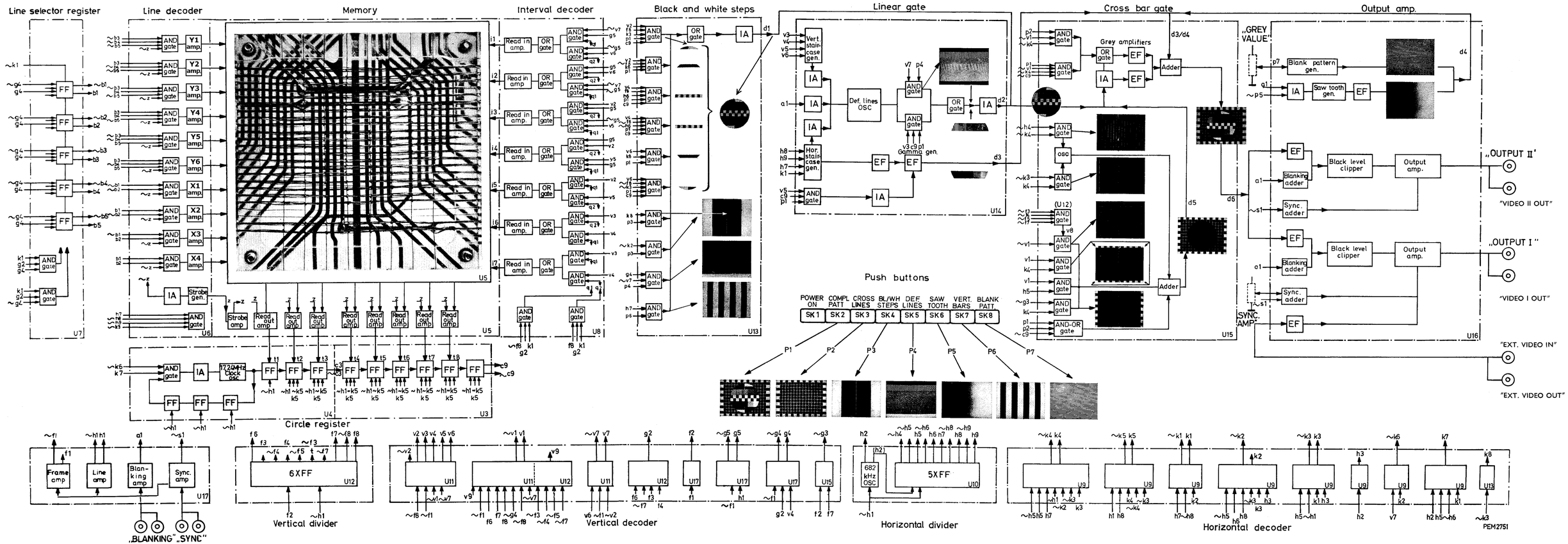


Fig. VIII-1 Detailed block-diagram

VIII Description of detailed block-diagram

The block-diagram is composed of 4 main groups:
- Input amplifiers
- Pulse generators (to control and drive the pattern generators)
- Pattern generators
- Output amplifiers.

Note:
In this block-diagram the pictures at the connections between units 13, 14, 15, and 16 are the ones present when button "COMPL. PATTERN" is depressed. Other signals will be present when one of the other push-buttons is depressed.

A. Input Amplifiers (part of U17)

The amplifiers have an high input impedance so that the input signals can be looped through without reflections.

B. Pulse Generators

They can be subdivided into 3 sections:
- Vertical divider and decoder
- Horizontal divider and decoder
- Generator for the circle-pulse.

1. Vertical Divider and Decoder

This section generates all the gating signals on a frame basis. The signals are obtained by counting down the line pulses ($\sim$ h1) in a 6-stage divider. The output signals from this divider are decoded to give the horizontal lines as well as the 8 intervals in vertical direction.

2. Horizontal Divider and Decoder

The line gating signals are derived from a 682 kHz oscillator, controlled by the line pulses. This oscillator signal is counted down in a 5-stage binary counter, the output signals of which are decoded to give the gating pulses in the horizontal direction.

3. Generator for the Circle pulse

The circle generator supplies 2 signals, "c9" and "$\sim$ c9", which are in anti-phase. The positive one, "c9", is used to emphasize the circle-area with the composite pattern, while the negative one, "$\sim$ c9", blanks the circle-area to make room for the composite circular pattern. The "c9"-pulses are obtained from a counting register that will count-down or forward the pulses from a 17.24 MHz clock-pulse oscillator. (Units 3 and 4)
The register is set for each line by pulses from a non-destructive ferrite core memory via 8 read-out amplifiers. The clock-pulse oscillator is started by "$\sim$ k6"-pulses and stopped by "k7"-pulses.
To ensure that the oscillator stops after a complete number of periods, the clock-pulse is fed back, via 3 flip-flops, to the and-gate, thus establishing a phase-lock.
By simultaneously supplying some cores with an X- and an Y-current (e.g. $X_1 + Y_2$) from the line decoder (unit 6), the memory is sensed line after line. The line decoder is controlled by the line-selector register (unit 7) that counts the "k1"-pulses, which are repeated in the middle of each line. The sensing moment of the cores is determined by the "$\sim$ z"-pulses originating from the strobe generator.
The memory consists of 22 $\times$ 8 cores and can, therefore, only contain information about 22 lines at the same time. As a result of this, after 22 lines (= one interval) the memory will receive new information about the next 22 lines from the interval decoder. This continues until all the 7 intervals, necessary to compose the circle, have been read-out. The interval decoder is controlled by pulses from the vertical and horizontal dividers and decoders.

C. Pattern Generators

They can be subdivided into 4 sections:
- Black and white steps
- Linear gate
- Cross-bar gate
- Blank pattern and sawtooth signal

1. Black and White Steps

When push-button "COMPL. PATTERN" is depressed, the first 6 and-gates (from the top) are producing parts of the circular pattern as shown in the block-diagram. As these gates are also controlled by the circle pulse (c9), they produce a pattern inside the circle-area only.

When push-button "BL/WH STEPS" is depressed, the 8th and-gate delivers the wide black bar on a blank pattern, while the 7th and-gate produces the thin white line in the middle of the black bar.

When push-button "DEF. LINES" is de pressed, the 9th and-gate produces a black picture with one horizontal white bar at the bottom for the definition lines test pattern.

When push-button "VERT. BARS" is depressed, the 10th and-gate produces a black picture with vertical white bars.

2. Linear Gate (Unit 14)

The generators deliver a horizontal and a vertical staircase signal, respectively.

When push-button "DEF. LINES" is depressed, the vertical staircase signal controls the definition lines oscillator to obtain a pattern containing 5 horizontal bars with definition lines.

When push-button "COMPL. PATTERN" is depressed, the horizontal staircase signal controls the definition-lines oscillator to obtain one horizontal bar with blocks of definition lines in vertical sequence. Besides it also controls the "gamma"-signal generator, to obtain one horizontal bar with a gamma signal. Because the appropriate circuits are also supplied with the circle pulse (c9), the said patterns are generated inside the circle area only.

3. Cross-Bar Gate

By means of a number of and-gates, several parts of the cross-bar pattern are generated.

The 3rd and-gate (from the top) produces the vertical white lines with the exception of the first one. The first vertical line is made in the 4th and-gate. Via a one-shot multivibrator, which determines the thickness of the lines (200 nsec.), both signals are fed to an adder circuit.

The 5th and 6th and-gate produce the horizontal white lines.

The 7th and 8th and-gates produce the black and white squares at the top and bottom of the pattern.

The 9th and-gate generates the black and white squares at the left – and right – hand side of the pattern.

All these signals are supplied to the adding circuit already mentioned.

The 10th gate, and the and/or gate, controls the adding circuit by means of the circle pulse ($\sim$ c9), thus blanking a black circle area out of the cross-bar pattern when push-button "COMPL. PATTERN" is depressed.

The grey amplifiers can each amplify only the pattern supplied to half of their white value. Together they produce a pattern with 100 % contrast.

The 1st and 2nd and-gate will, via an or-gate, control one of the amplifiers during the moments the pattern should be grey.

In an adding circuit, parts of the various patterns are added and applied to the output amplifiers (unit 16).

4. Blank Pattern and Sawtooth Signal

On the printed wiring board of the output amplifiers a blank pattern-"generator" is mounted, the contrast-level of which can be adjusted with a potentiometer at the front of the apparatus. Moreover, a sawtooth generator producing a pattern, changing linearly from black to white, is also mounted on this unit. Both signals are fed to the adding circuit of unit 15.

D. Output Amplifiers

Both video outputs ("I" and "II") are fed by more or less identical circuits, containing, among others, a black level clipper and an output amplifier with low output impedance (75 Ω). By means of additional circuits, the complete synchronizing and blanking signals are added.

The input circuit of amplifier I contains a potentiometer that enables the video signal (excl. sync.) at output I to be adjusted between 0.5 and 1 $V_{p\text{-}p}$ thus giving a possibility to vary the mixing-ratio of the internal pattern and a synchronized video signal connected to socket "EXT. VIDEO".

Moreover, it is possible to vary the sync. amplitude of the signal at output I between 0 and 200 % with control "SYNC. AMPL." on the front panel.

The circuit of amplifier II does not provide the above mentioned control of the signals, neither can an external video signal be added, in this case.

SERVICE INSTRUCTIONS

In the following chapters the circuitry of the units has been explained. The service-adjustments have been described at the end of the chapter concerned.

Please bear in mind the following notes:

- The unit to the checked or adjusted, should be placed on the "EXTENSION BOARD", unit 2 of the instrument.
- terminate parallel sockets with 75 Ω.
- Apply the complete sync. signal to socket "SYNC-" and the complete blanking signal to socket "BLANKING-". These signals are derived from the PHILIPS TV-pulse generator PM 5530.
- The tolerances mentioned are factory tolerances which apply when-adjusting the instrument. They may differ from those shown in section "GENERAL", chapter "TECHNICAL DATA".
- The voltages shown in the diagram and the oscillograms published are measured with respect to terminal 12 (instrument connected to 220 V~).
- The d.c. voltages are measured with a PHILIPS d.c. voltmeter PM 2430.
- The a.c. voltages on unit 1 are measured with a PHILIPS a.c. voltmeter PM 2451.
- The oscillograms are measured with a PHILIPS oscilloscope PM 3330 in connection with a PHILIPS double trace unit PM 3342 and a PHILIPS time base delay unit PM 3347.
- The oscillograms are photographed with a PHILIPS camera outfit PM 9300.

N.B. Disconnect the mains before exchanging printed wiring units!

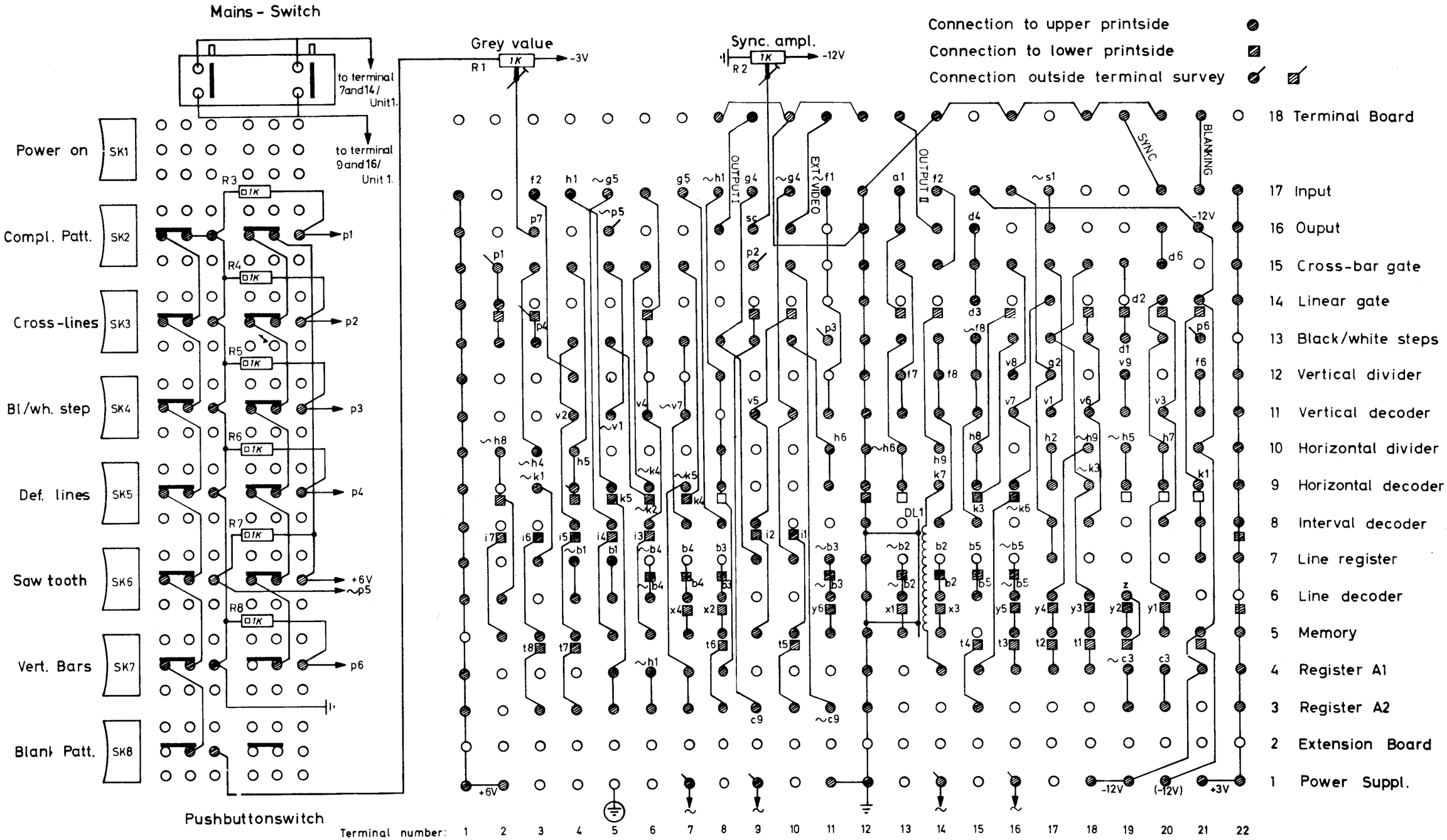


Fig. IX-1 Connection-terminal blocks

IX Unit 1

The power supply unit

The power-supply unit contains 3 stabilized rectifiers for the voltages –12 V, 6 V and 3 V.
The primary of the mains transformer has two separate windings (S1 + S2). They are connected in series when the apparatus is to be used with 230 V mains (± 20 %) and in parallel in case of 115 V mains (± 20 %).

The 12-Volt rectifier

The voltage from winding S4 (17V) is rectified in diodes GR2 and stabilized by TS13. This transistor, which acts as a variable resistor, is so controlled that the –12 Volt output (terminals 18-19) is kept constant. The control current for TS13 is supplied by TS14 which is controlled by TS7. Here the emitter voltage is kept constant by Zener diode GR6. The base voltage of TS7 is dependent on the output voltage across R30, R29 and R31. If, for instance, this voltage becomes more negative, the emitter-base voltage of TS7 also becomes more negative, which, via emittor follower TS4, causes the current through TS13 to decrease.
This counteracts the voltage increase across R29-R30. The –12 Volt is adjusted by selecting the correct value of R31. TS1 operates as an overload protection. The base-emitter voltage is so selected by R8 that TS1 is cut-off. But if overloading takes place, the voltage across R11 increases and the emitter-base-voltage decreases, so that TS1 becomes conductive and the current through TS13 decreases.
The current for changing the magnetic state of the ferrite cores of the memory (approx. 800 mA) is taken from the –12 Volt (terminal 20). This current is tapped via TS12. TS12 has a heavy DC-feedback via R39. The AC-impedance is high due to the base decoupling of C5, which prevents the –12 Volt from being influenced by the strong current pulses.

The 6-Volt rectifier

The rectifying, stabilizing and the overload protection are the same as in the –12 Volt rectifier, only the control of the voltage variation is different. Here, the reference voltage is produced across the common emitter resistor R27. This voltage is kept constant by the current through TS9, which is stabilized by Zener diode GR7. The base voltage of TS8 is dependent on the output voltage across R21, R22 and R23. The overload protection is effected by TS2 and is adjusted by R9.

The 3-Volt rectifier

This rectifier is built up as the 6-Volt rectifier. On account of the low output voltage, the base of TS11 is dependent on the voltage across R33, R35, R36 and Zenerdiode GR8. The 3-Volt output is adjusted by selecting the correct value of R33. Resistor R10 is selected for the overload protection of TS3.
The collector voltage of TS7 . . . TS11 is produced by GR1 and stabilized by Zenerdiode GR5.

Checking and adjusting

Measuring equipment:
D.C. voltmeter: e.g. PHILIPS PM 2430.
Oscilloscope: e.g. PHILIPS PM 3230.
The stabilized voltages should not change more than 0.2 % with mains voltage variations of 180 to 280 V and 92 to 135 V respectively.
The following checks and adjustments are to be carried out at nominal mains voltage.
Push-button switch SK2 "COMPL. PATTERN" depressed.
Terminate "EXT. VIDEO OUT" with 75 Ω.

+ 6 V: this voltage is adjusted by selecting R23 (10 Ω – 470 Ω)
+ 3 V: this voltage is adjusted by selecting R33 (560 Ω – 4.7 kΩ)
– 12 V: this voltage is adjusted by selecting R31 (2.7 kΩ – 15 kΩ).

The base-emitter voltage of TS1 . . . TS3 should be 200 mV, – 20 % + 10 %.
This voltage is adjusted by selecting R8 (220 Ω – 820 Ω), R9 (150 Ω – 1.5 kΩ) and R10 (330 Ω – 4.7 kΩ) respectively.
Check the ripple voltages at a mains voltage of 180 V (voltage selector in position "230 V").

At + 6 V:
+ 3 V:
– 12 V: } $< 2\ mV_{pp}$ (without signals from a PM 5530)

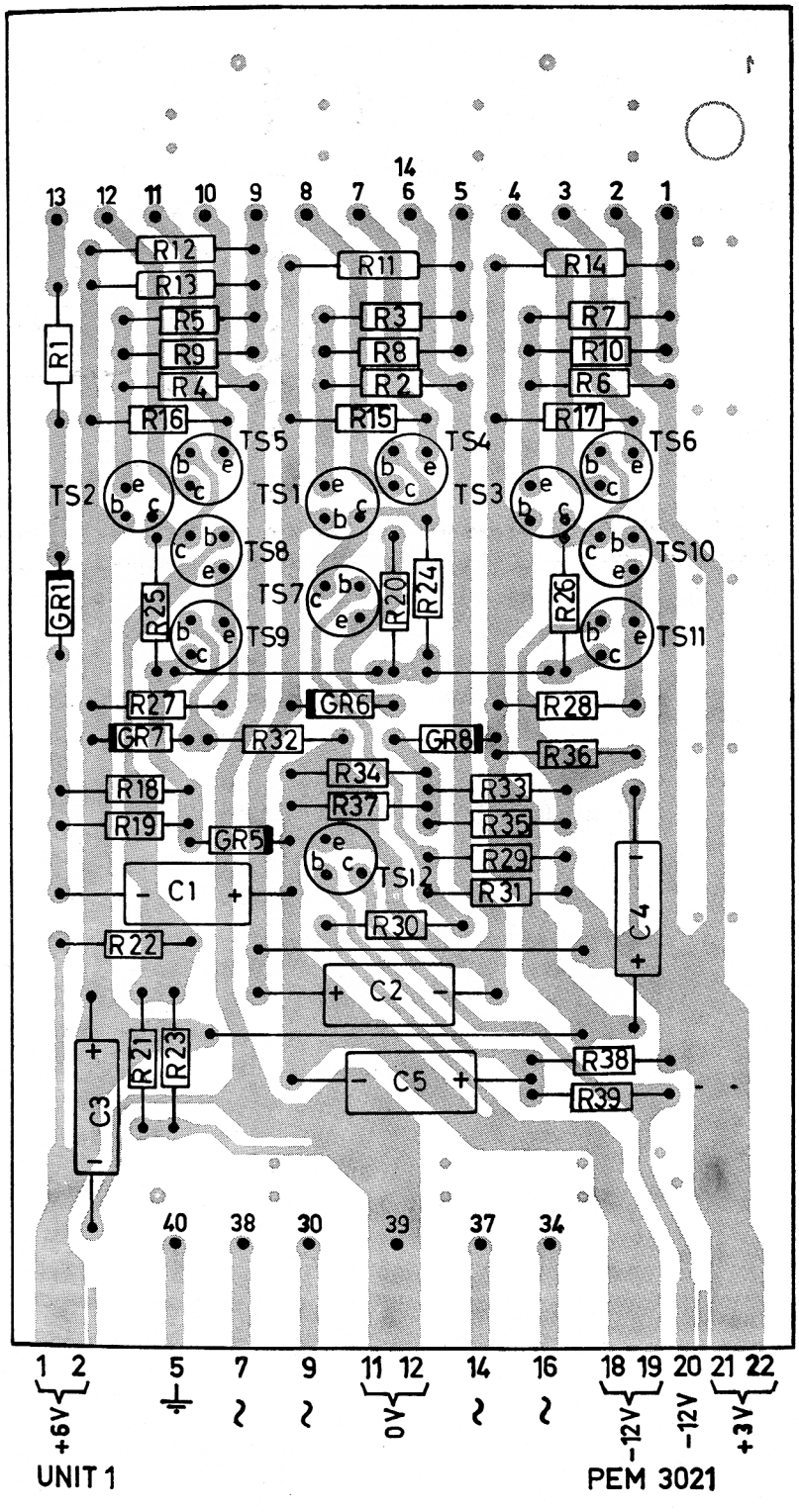


Fig. IX-2 Printed wiring board, Power supply, Unit 1

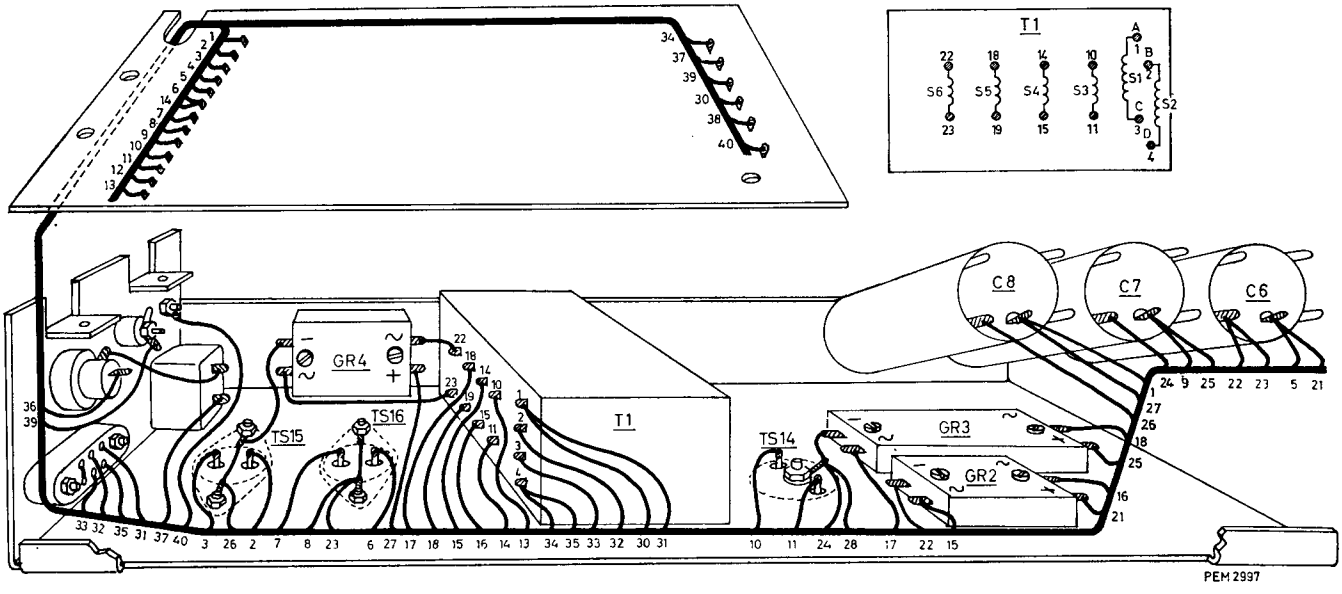


Fig. IX-3 Wiring power supply

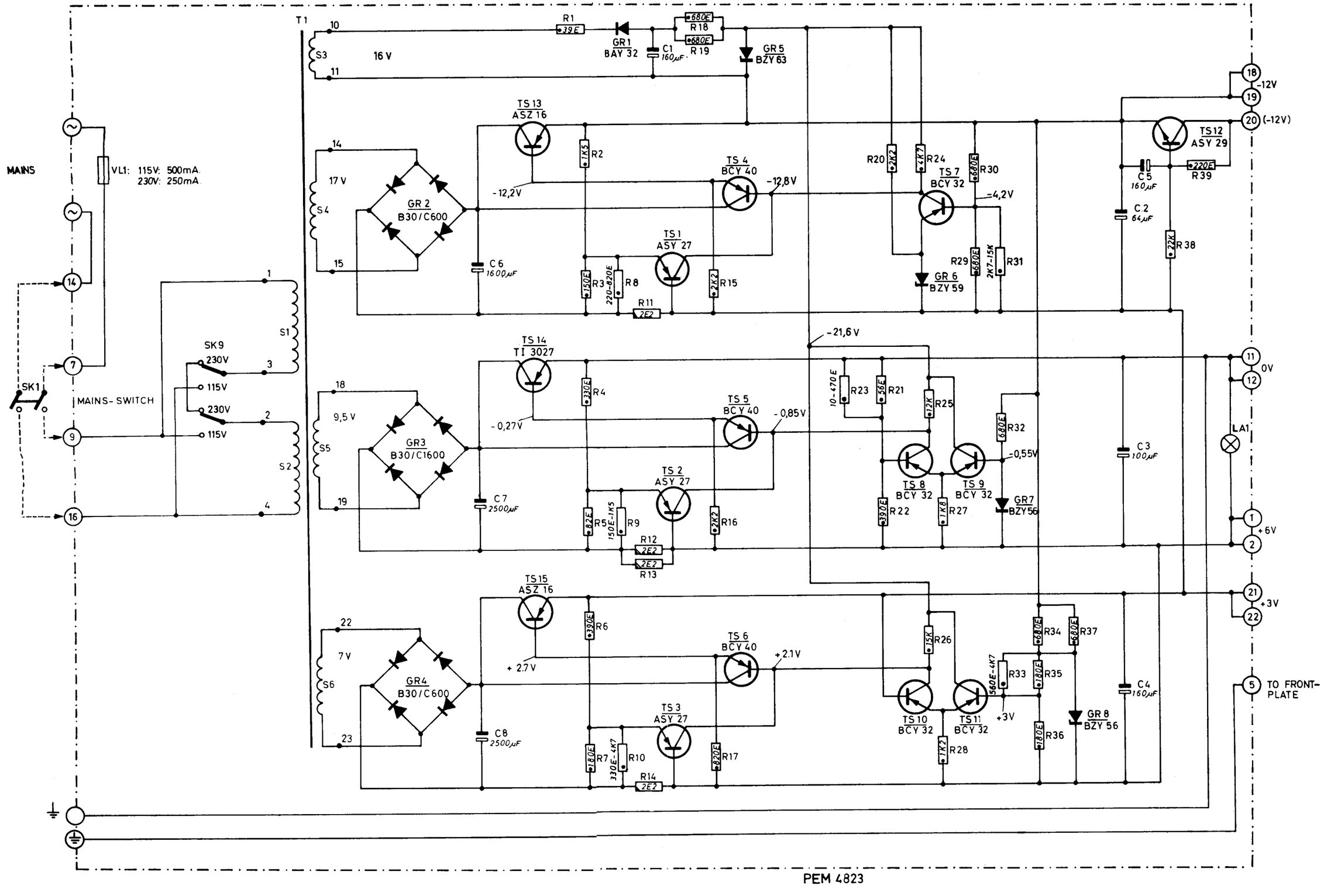


Fig. IX-4 Circuit diagram, power-supply, Unit

From version /06 a resistor of 47 Ω -¼w-5% is connected in series with the pilot lamp LA1.

X Units 3 and 4

The circle register

The circle register is accommodated on units 3 and 4. It consists of a 17 MHz clock-pulse oscillator and an 8-bit counting register for generating the circle informations.

The 17 MHz clock-pulse oscillator (unit 4)

Transistors TS1 and TS2 form an emitter-coupled oscillator.

The frequency is dependent on the value of R4 and R6. The circle register is controlled by the output voltage of the oscillator, which is taken from the collector of TS2.

The "∿ k6" pulse actuates the oscillator within the periods limited by the envelope of the circle, while the "k7d" pulse stops and starts the oscillator during the periods the counting sense of the register is reversed. The counting sense of the register is reversed at the centre of the circle. This means that the register is in a well-defined state when the clock-pulse oscillator is stopped. The oscillator is stopped after an exact number of oscillations.

This is effected by means of the 3-bit divider CB1 . . . CB3 which supplies only one output pulse every eight oscillator-clock pulses.

Just before the centre line, the 31st output pulse of CB3 is selected by the "k7d" pulse, which determines the stop and start of the oscillator. The oscillator is stopped after the 31st output pulse of CB3 with a small delay. This delay is determined by the 8 : 1 divider CB1 . . . CB3 (8 × 31 = 248 periods), and a small constant delay of OR-gate GR8 . . . GR10 and transistors TS3 and TS4.

The oscillator is started again at the trailing edge of the "k7d" pulse (see Fig. X-2).

The counting register

The eight-bit register consists of the circuit blocks CB4 . . . CB6 in unit 4 and CB1 . . . CB6 in unit 3.

It can be set to zero (reset), set to down or forward-counting and set by means of the read out pulses from the memory (preset).

The function of the register is a follows:

At the beginning of a line the register is set zero by the "∿ h1" pulse. The counting direction of the register is determined by the "k5" and "∿ k5" pulses so that it is down-counting up to point C (see Fig. X-1).

Before the clock-pulse oscillator starts, the read-out pulses t1 . . . t8 of the memory are applied to the register via C23 . . . C25 in unit 4 and C25 . . . C29 in unit 3.

At point A (Fig. X-1) the clock-pulse oscillator is started by the "∿ k6" pulse. At the same time the register is set to down-counting by the read-out digit from the memory, which has been set into the register. When the register passes zero circuit block CB6 delivers the "c9" an "∿ c9" pulses. The leading edge of this pulse corresponds to the front envelope of the circle "B" (Fig. X-1). Just before the centre line "C" (Fig. X-1) the clock-pulse oscillator is stopped as described above. Then the counting direction of the register is reversed to forward-counting by the "k5" and "∿ k5" pulses and the clock-pulse oscillator is started again by the trailing edge of the "k7d" pulse (see Fig. X-2). The register then counts forwards to zero during the right half of the circle. When again passes zero it will have counted exactly the same number of periods as during the left half of the circle. When passing zero circuit block CB6 delivers the trailing edge of the "c9" and "∿ c9" pulses which correspond to the back envelope of the circle "D" (Fig. X-1). The "c9" and "∿ c9" pulses are applied to the units 13, 14 and 15 to be combined with the rest of the test pattern.

Checking and adjusting

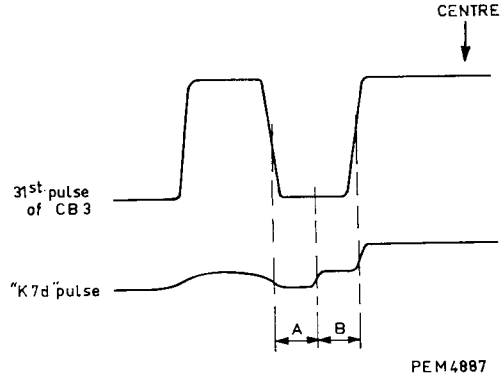
Measuring equipment:

Oscilloscope	e.g. PHILIPS PM 3330
With dual-trace-Y amplifier	e.g. PHILIPS PM 3342
Monitor	e.g.

Clock-frequency (approx. 17 MHz)

Connect the A amplifier of the oscilloscope to point 1 of CB3 and the B amplifier to terminal 17.

Trigger with the "h1" pulse (terminals 4 of unit 17) and display the centre of the T.V. line.
The oscillogram should be as shown in the figure below.
The width of A and B should be equal.
If not, select another value for R6 (10 kΩ . . . 47 kΩ).



Position of the front envelope of the circle
Connect the monitor to BU5 (BU2) "VIDEO II OUT". Adjust the monitor so that the complete pattern is displayed. The circle should start exactly at the transient of the black-white steps in the middle of the circle. If not, select another value for R32 in unit 9 (4.7 kΩ . . . 12 kΩ).

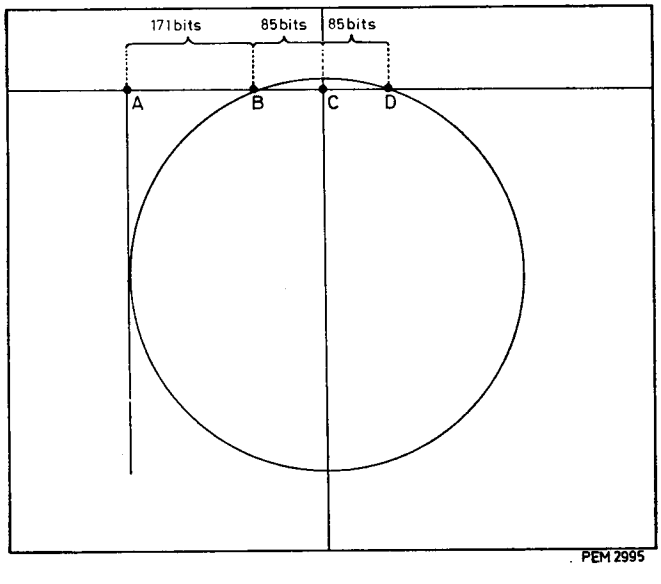


Fig. X-1 Circle

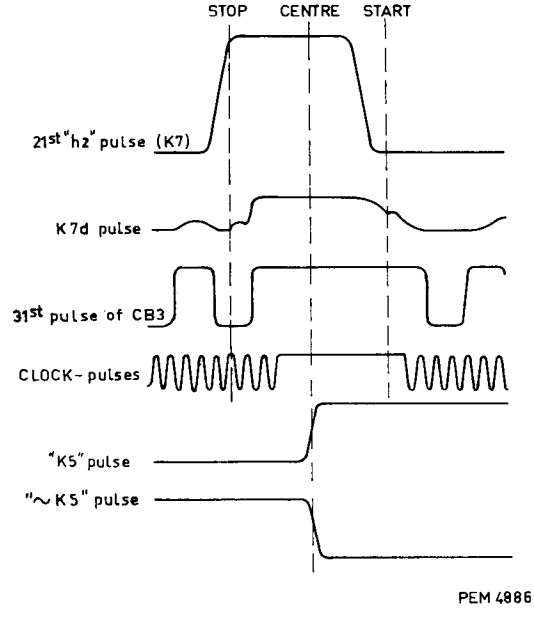
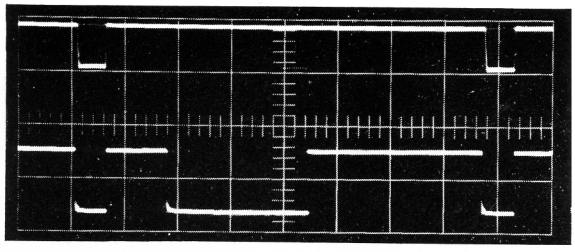
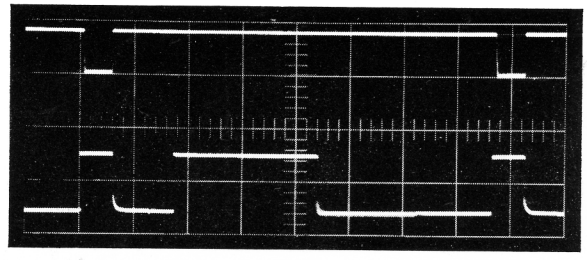


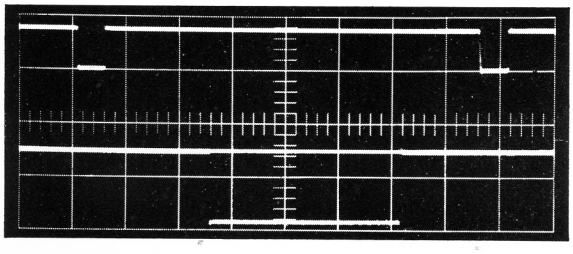
Fig. X-2 Pulse diagram



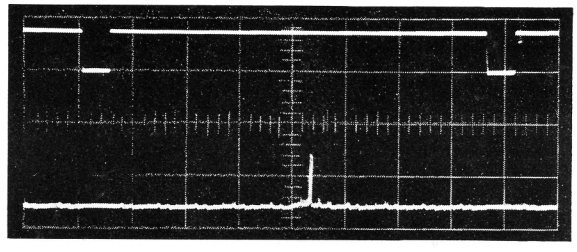
k5
5 V/cm 8 µs/cm
reference: line sync.



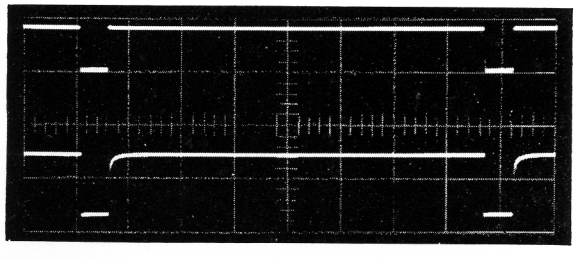
~ k5
5 V/cm 8 µs/cm
reference: line sync.



~ k6
1 V/cm 8 µs/cm
reference: line sync.



k7
1 V/cm 8 µs/cm
reference: line sync.



~ h1
5 V/cm 8 µs/cm
reference: line sync.

Fig. X-3 Oscillograms, Units 3 and 4

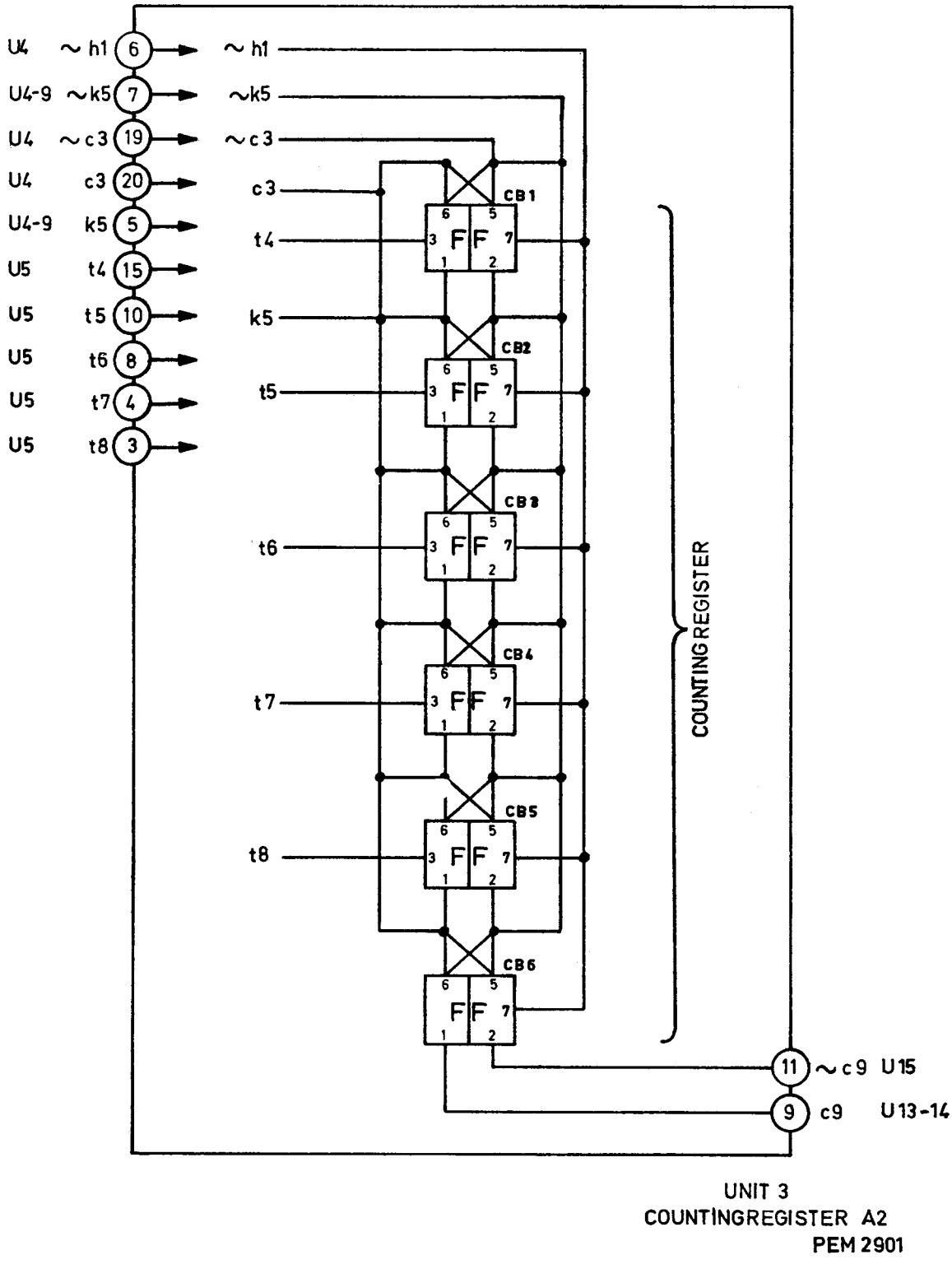


Fig. X-4 Block-diagram, counting register, Unit 3

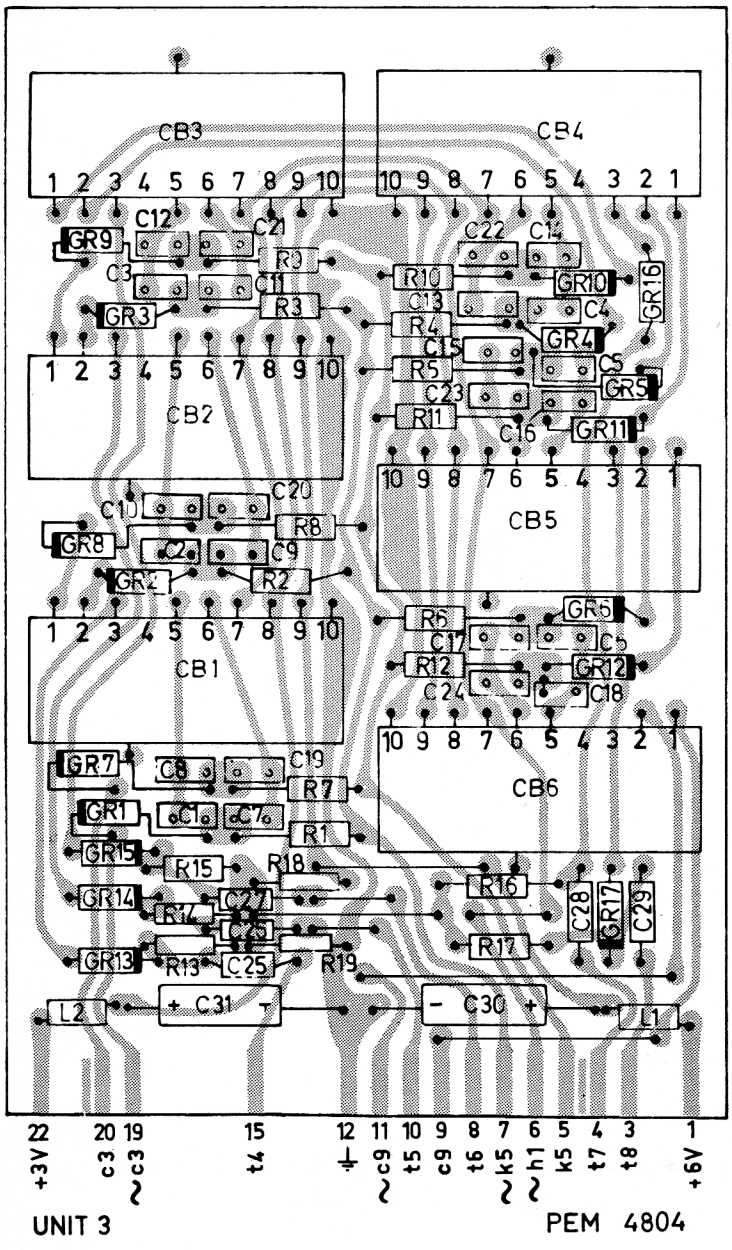


Fig. X-5 Printed wiring board, counting register, Unit 3

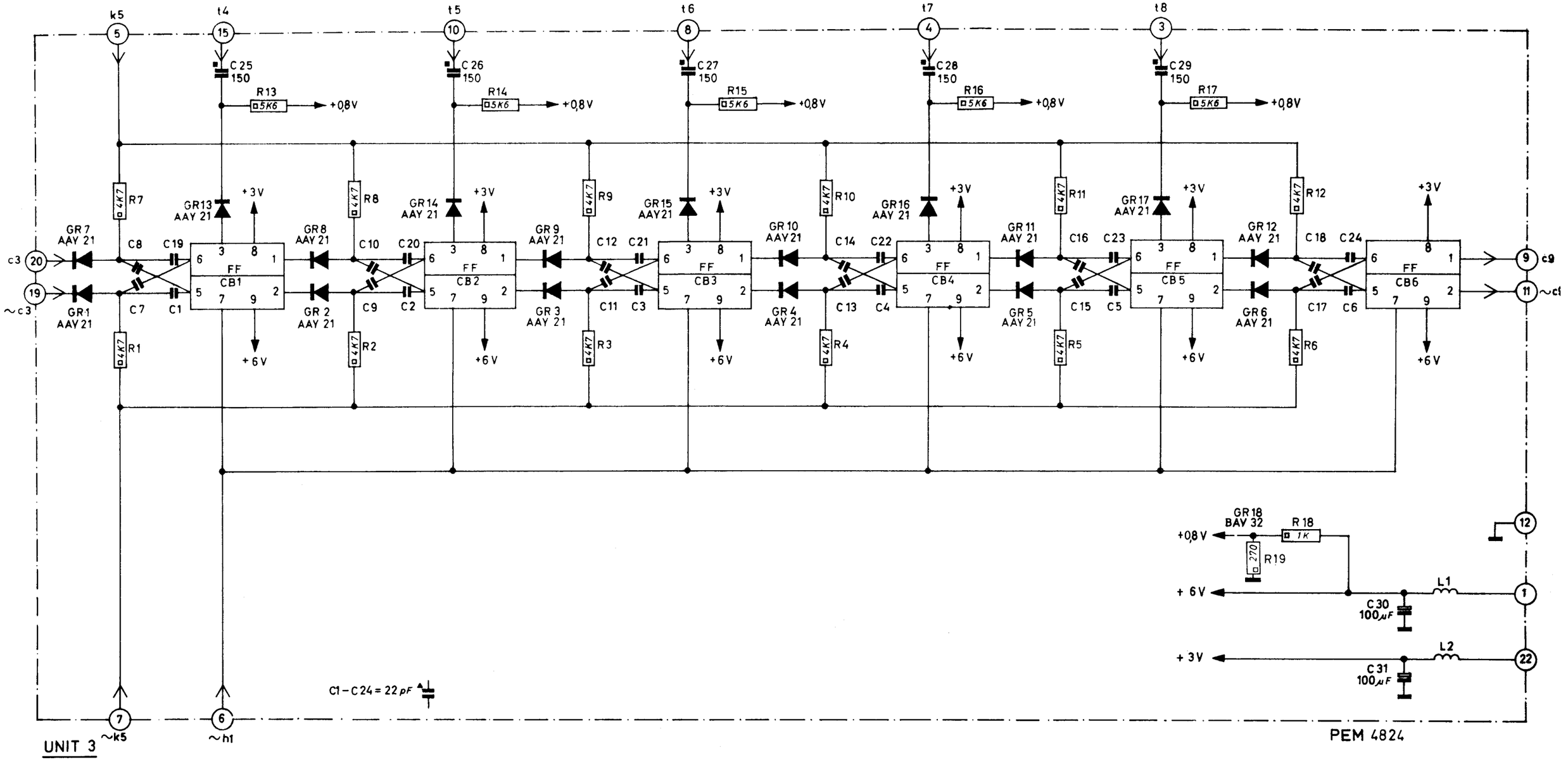


Fig. X-6 Circuit diagram, counting register, Unit 3

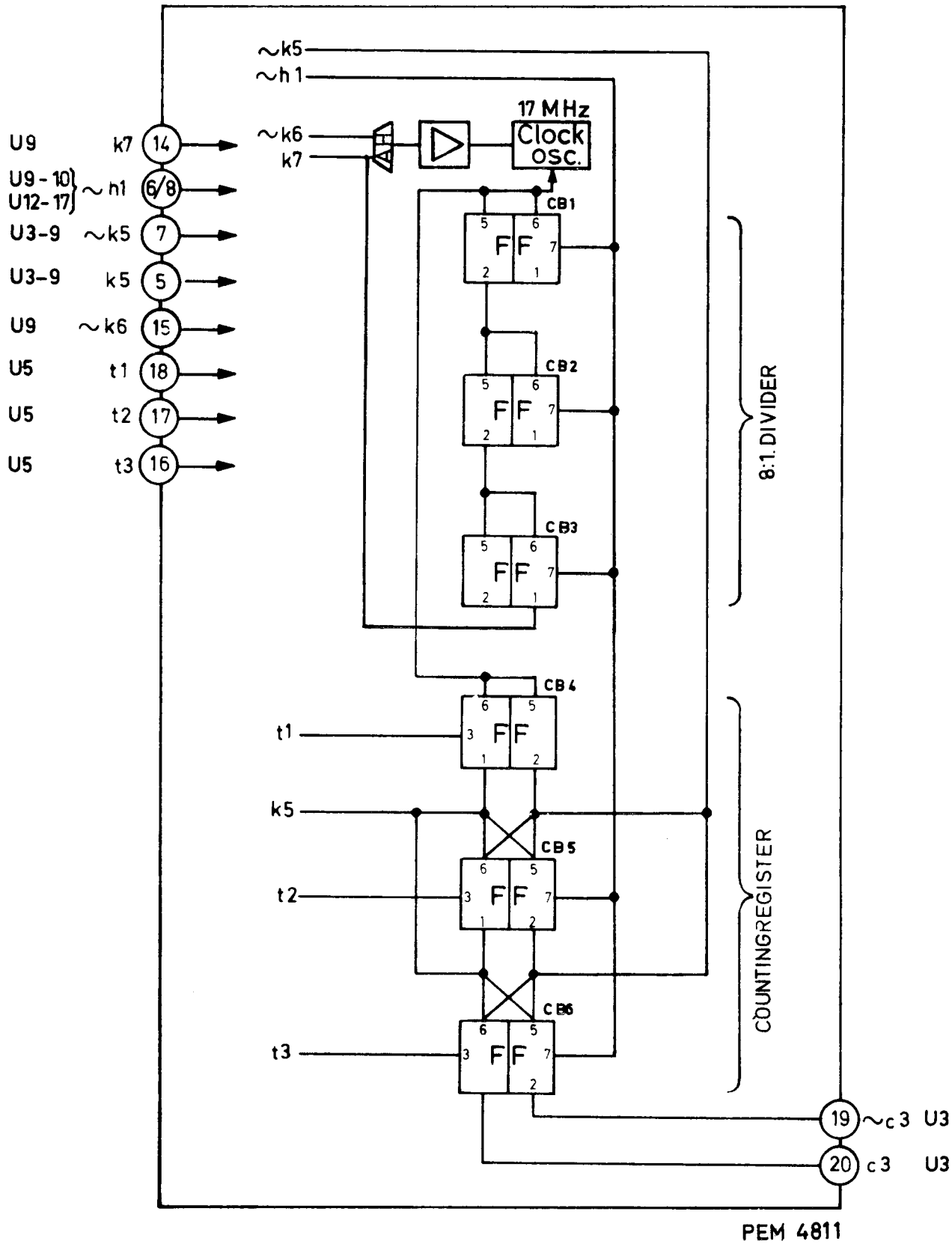


Fig. X-7 Block-diagram, circle register, Unit 4

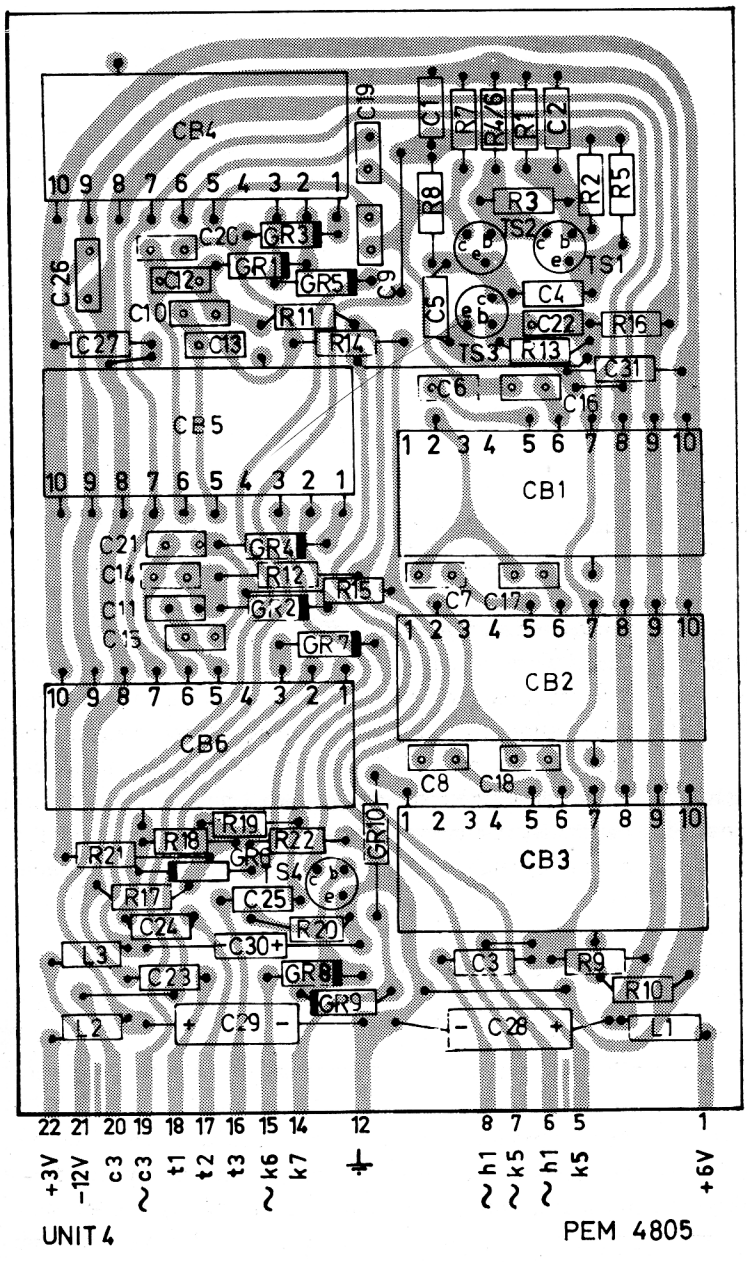


Fig. X-8 Printed wiring board, circle register, Unit 4

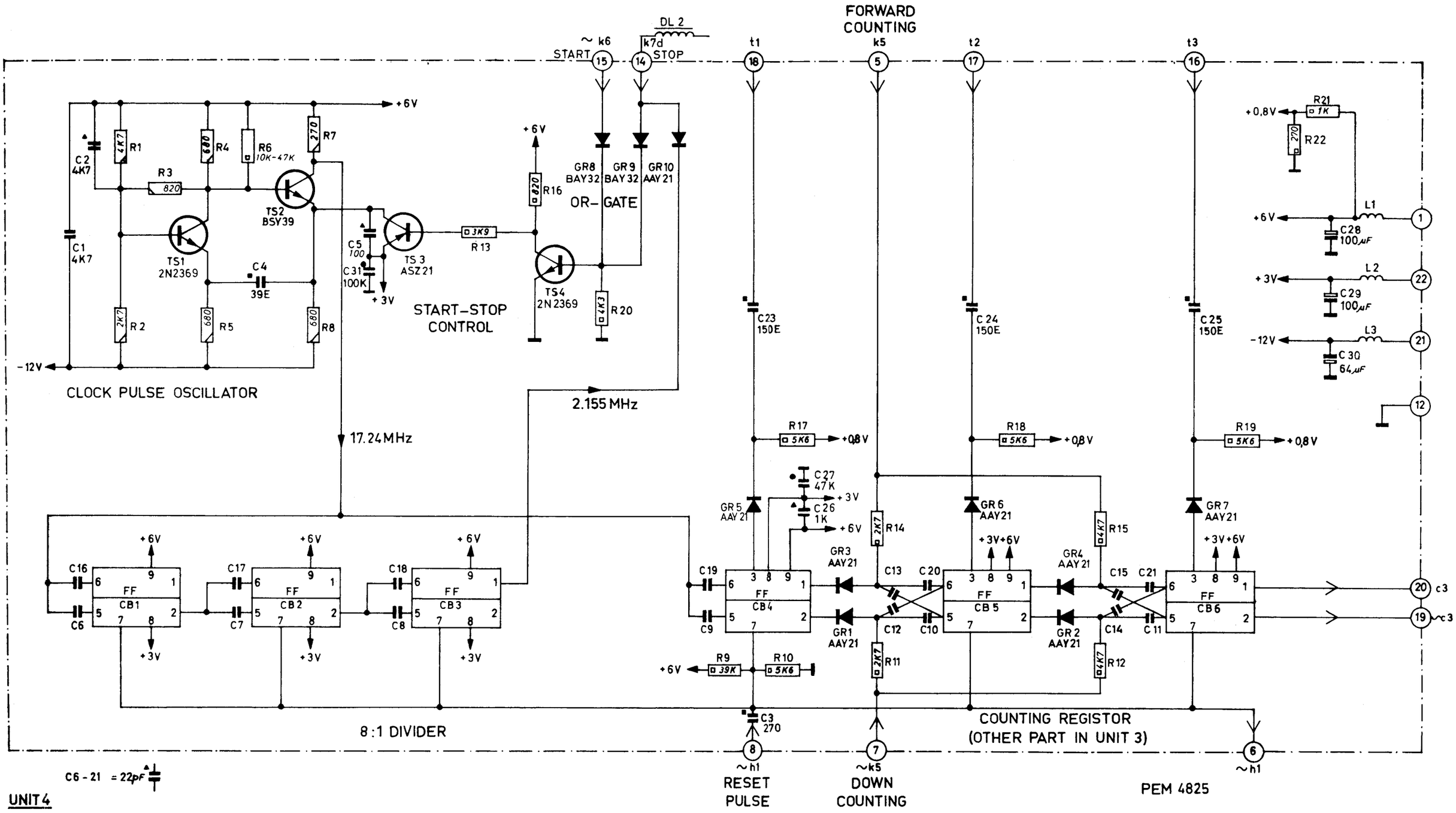


Fig. X-9 Circuit diagram, circle register, Unit 4

XI Unit 5

The memory

The memory consist of a ferrite core matrix, the read-out circuits TS1 . . . TS8 and strobe amplifier TS9.

The ferrite core matrix

Each interval covers 22 lines, while the information for each line is a binary figure of 8 bits. The memory is formed as a matrix of 22 lines, each containing 8 ferrite cores.

These cores are, from line to line, turned 90° to obtain read-out pulses with the same polarity at the vertical read-out wires.

The interval read-in wires (i1 . . . i7) pass the cores where the binary figure should be "1", and by-pass them if the figure should be "0" (see Fig. XI-1). Each line consist of line-selector wires X1 . . . X4 and Y1 . . . Y6. Each wire is driven with half current pulses in the same phase so that each of these combinations can select one line.

With the four X-wires and the six Y-wires 24 combinations are possible, which represent a selection of 24 lines (French system). However, for the 625-lines system the first 22 combinations are used, while for the 525-lines system only the first 18 combinations are used.

Before a read-in takes place, all cores are automatically set to zero by the preceding read-out pulse.

On reading-in a current flows through one of the 7 selected interval wires (i1 . . . i7) to reverse the magnetic state of the corresponding cores. The cores not being passed, are not set.

The reading-in of a new interval is made at the moment that the middle of the last line of the preceding interval is produced by the circle register.

At the beginning of each line of an interval, the half-current pulses, which pass through the X and Y-line selector wires, cannot separately cause the cores to reverse their magnetic state. If these half-current pulses in both wires coincide, they set the cores of the line concerned to zero. When the cores are set to zero, a voltage on the vertical read-out wires is induced and passed on to the read-out amplifiers TS1 . . TS8. After amplification and pulse shaping the latter supply the pulses "t1 . . . t8" which are used for setting the respective flip-flops of the counting register (units 3 and 4). At the beginning of the next line the X- and Y-wires again carry half-current pulses, so that the information for this line is also transferred to the counting register. This process is repeated line after line until all information for the 22 lines is transferred. At the middle of the 22nd line, the information of the next interval is read in and the setting to zero is made.

The read-out amplifiers

These amplifiers are transformer-coupled to the read-out wires by T1 . . . T8.

The ratio is 1:10 and directed so that the read-out pulses saturate the succeeding transistors TS1 . . . TS8. As the read-out wires are threaded through all cores, all induced signals are amplified. This implies that the unwanted signals from the cores through which only half-current pulses are flowing will also be amplified and create false pulses. However, because of the non-linear hysteresis loop of the cores only the full current pulses are delayed about 0.75 µs. So these correct pulses will be separated from the false ones by the gating of strobe amplifier TS9.

The "z" pulse, originating from the strobe generator (U6), is also delayed 0.75 µs by C1-R20 and saturate TS9. When TS9 is saturated, the base levels of TS1 . . . TS8 are at emitter level of TS9 and as a result of this TS1 . . . TS8 are actuated by positive going pulses from the transformers.

During this time negative going pulses (t1 . . . t8) appear at the collectors of TS1 . . . TS8. These pulses are used for setting the counting register in units 3 and 4.

Checking and adjusting
Measuring equipment:
Oscilloscope: e.g. PHILIPS PM 3330.

Read- in currents (i1 . . . i7)
Connect the oscilloscope across R22-R23. Check that the individual pulses are approx. 11 V_{p-p} (corresponding to approx. 755 mA – 800 mA).
If not, select R23 (68 Ω – 150 Ω). If the control range of R23 is not sufficient check the corresponding read-in amplifier (unit 8).

Read- in currents (X and Y)
Connect the oscilloscope across R24-R25 for the Y pulse and across R26-R27 for the X pulse. Check that the individual pulses are between 13.5 V_{p-p} and 14 V_{p-p} (corresponding to approx. 380 – 400 mA). If not, select R25 (270 Ω – 470 Ω) for the Y pulses and R27 (270 Ω – 470 Ω) for the X pulses. If the control ranges of these resistors are not sufficiënt, check the corresponding read-in amplifier (unit 6).

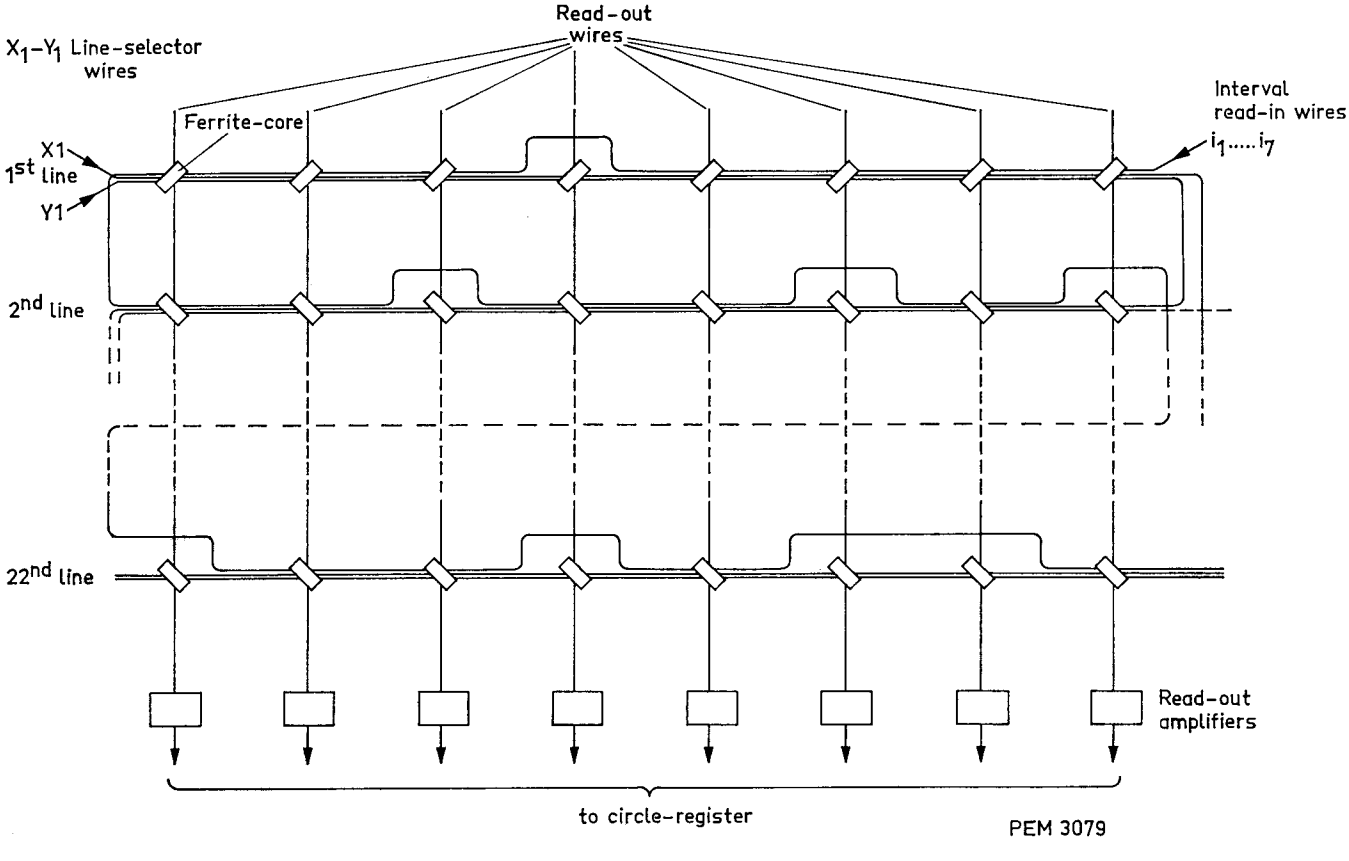


Fig. XI-1 Principle of the memory

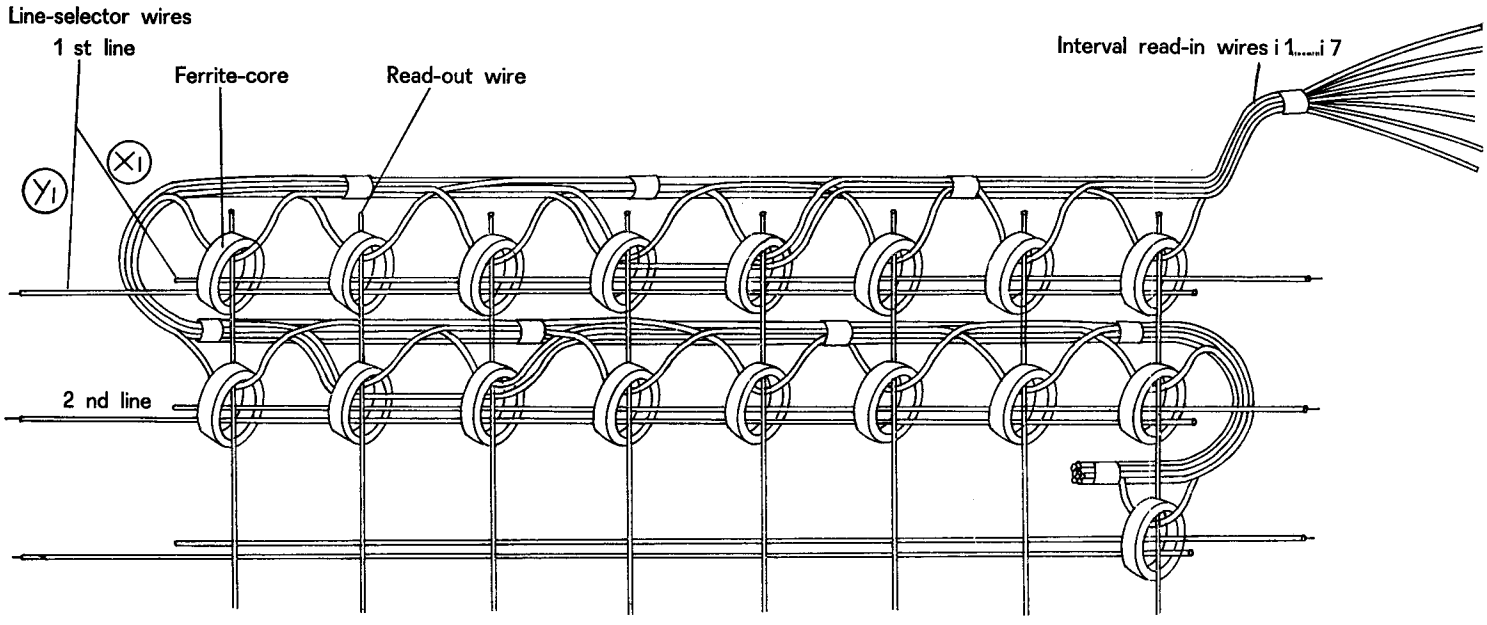


Fig. XI-2 Wiring diagram of the memory

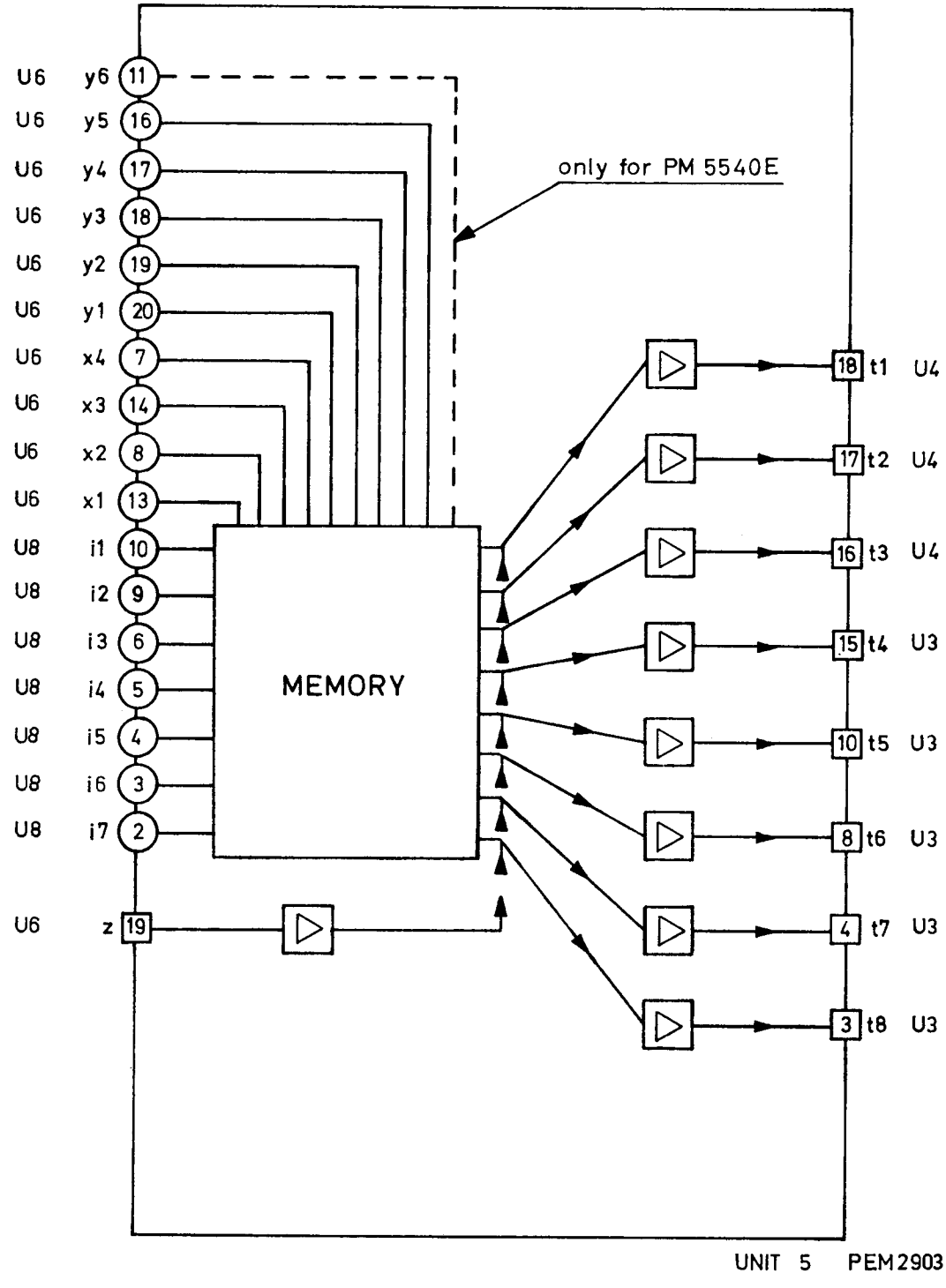


Fig. XI-3 Block-diagram, memory, Unit 5

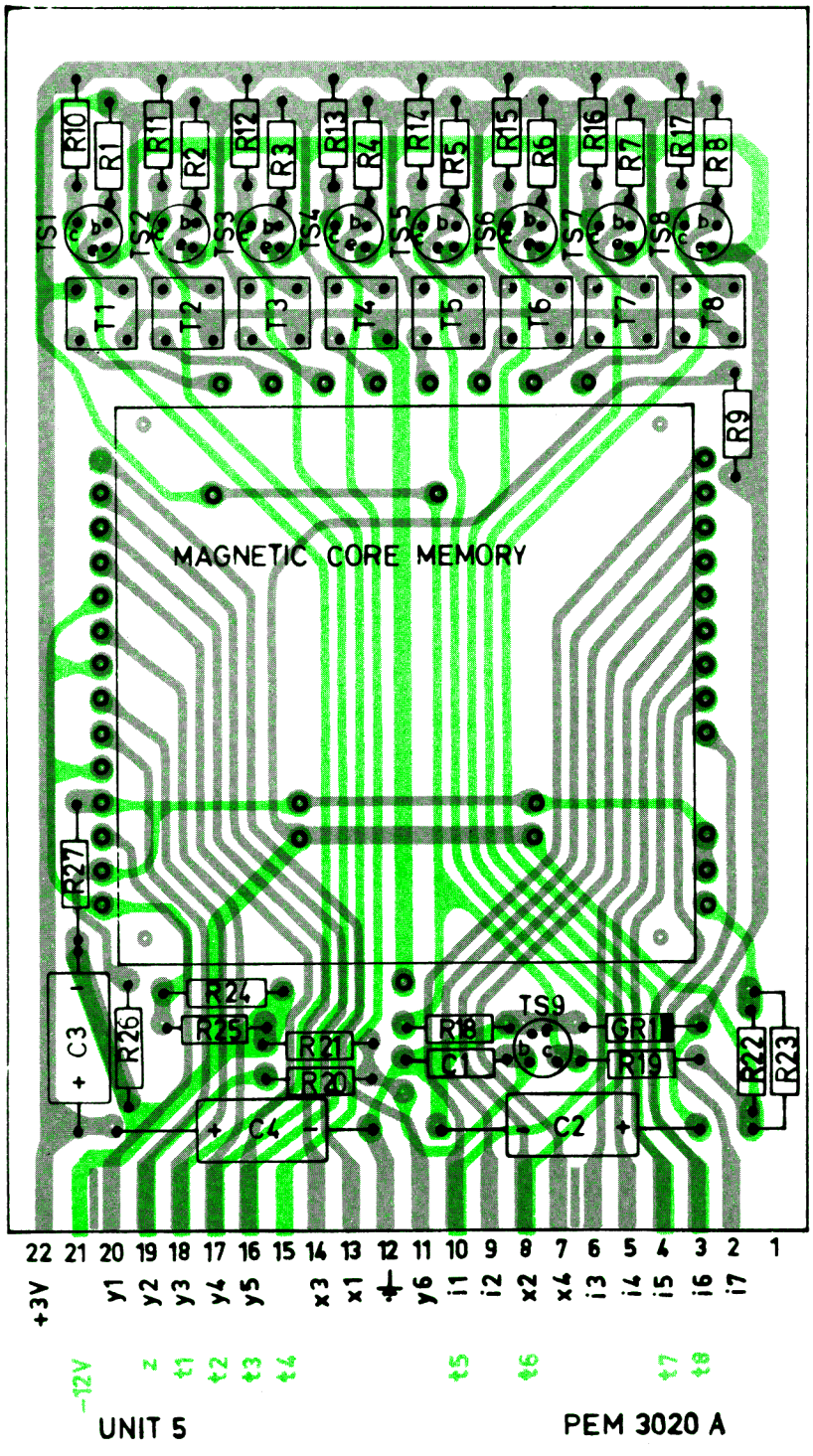


Fig. XI-4a Printed wiring board, memory (A version), Unit 5

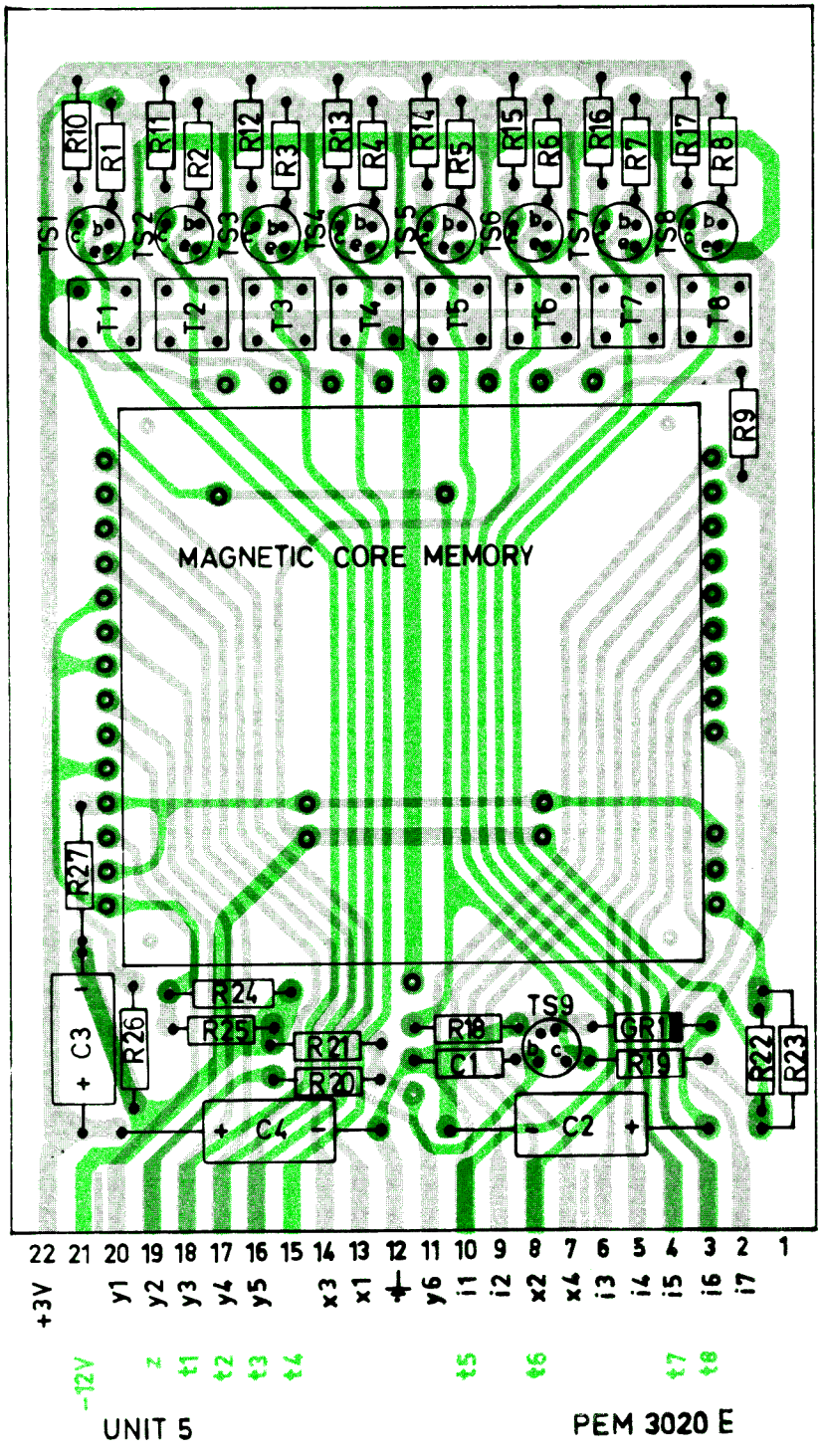


Fig. XI-4b Printed wiring board, memory (E version), Unit 5

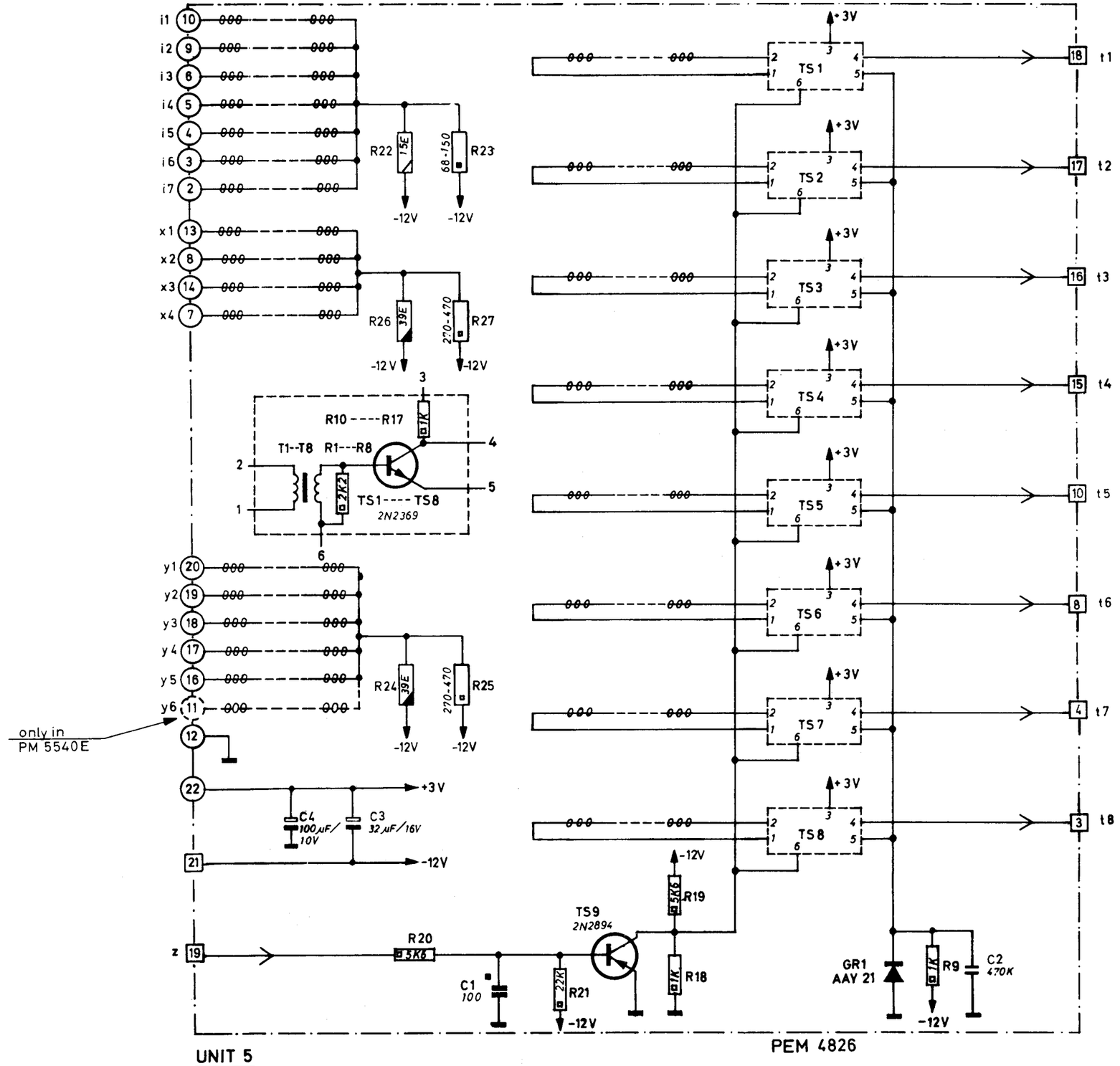


Fig. XI-5 Circuit diagram, memory, Unit 5

From version /06 the following is modified:
— GR1 is of the type AAZ15 (4822 130 30229)
— C1 has become 150pF

XII Unit 6

The line decoder

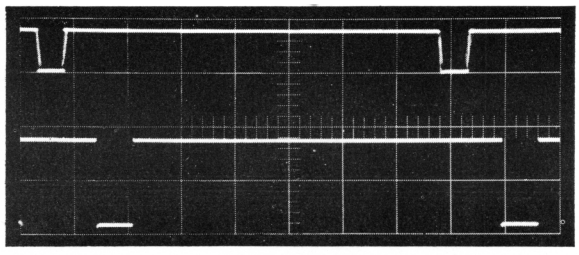
The decoder consists of the AND-gates GR27 . . . GR38 for the X-read-in pulses and the AND-gates GR7 . . . GR26 and GR39 . . . GR42 for the Y-read-in pulses.
These gates are succeeding by the read-in amplifiers TS3 . . . TS22. The read-in current is about 400 mA.
In the AND-gates, the X- and Y-pulses are produced by combining the pulses from the flip-flops of the line selector register.
The table below shows the composing of the X- and Y-pulses for reading- in the 22 lines.

Strobe generator
This circuit consists of an AND-gate GR1 . . . GR4 and the amplifiers TS1 and TS2.
In the AND-gate the "z" pulse is produced by combining suitable pulses from the horizontal divider (unit 10) and the horizontal decoder (unit 9).
The "z" pulse is transferred to the strobe amplifier in unit 5, while the "$\sim$ z" pulse is used for control of the X and Y AND-gates.

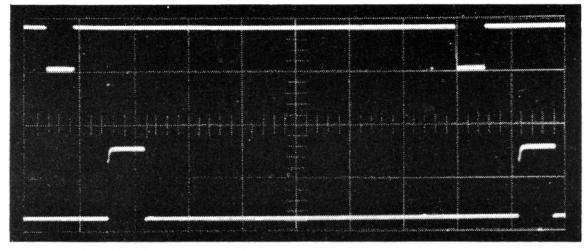
Line selector register

number	CB5	CB4	CB3	CB2	CB1	x_1	x_2	x_3	x_4	y_1	y_2	y_3	y_4	y_5	y_6*
1	0	0	0	0	0	1				1					
2	0	0	0	0	1		1			1					
3	0	0	0	1	0			1		1					
4	0	0	0	1	1				1	1					
5	0	0	1	0	0	1					1				
6	0	0	1	0	1		1				1				
7	0	0	1	1	0			1			1				
8	0	0	1	1	1				1		1				
9	0	1	0	0	0	1						1			
10	0	1	0	0	1		1					1			
11	0	1	0	1	0			1				1			
12	0	1	0	1	1				1			1			
13	0	1	1	0	0	1							1		
14	0	1	1	0	1		1						1		
15	0	1	1	1	0			1					1		
16	0	1	1	1	1				1				1		
17	1	0	0	0	0	1								1	
18*	1	0	0	0	1		1							1	
19*	1	0	0	1	0			1						1	
20*	1	0	0	1	1				1					1	
21*	1	0	1	0	0	1									1
22*	1	0	1	0	1		1								1

*) Not in PM 5540 A



z
2 V/cm 8 µs/cm
reference: line sync.



~ z
2 V/cm 8 µs/cm
reference: line sync.

Fig. XII-1 Oscillograms, Unit 6

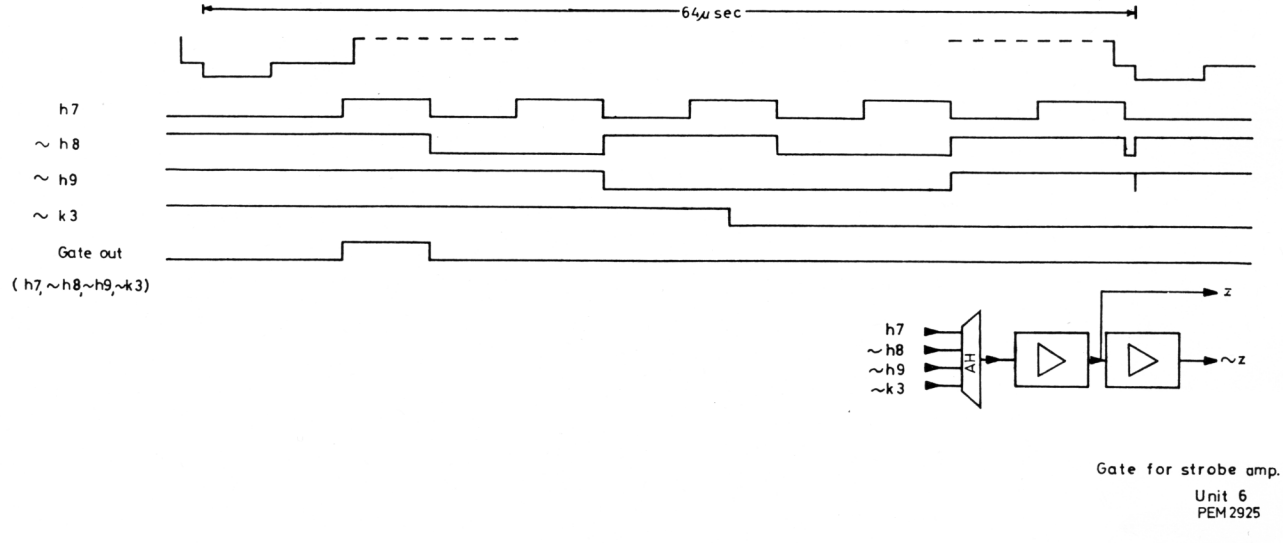


Fig. XII-2 Gate for strobe amplifier

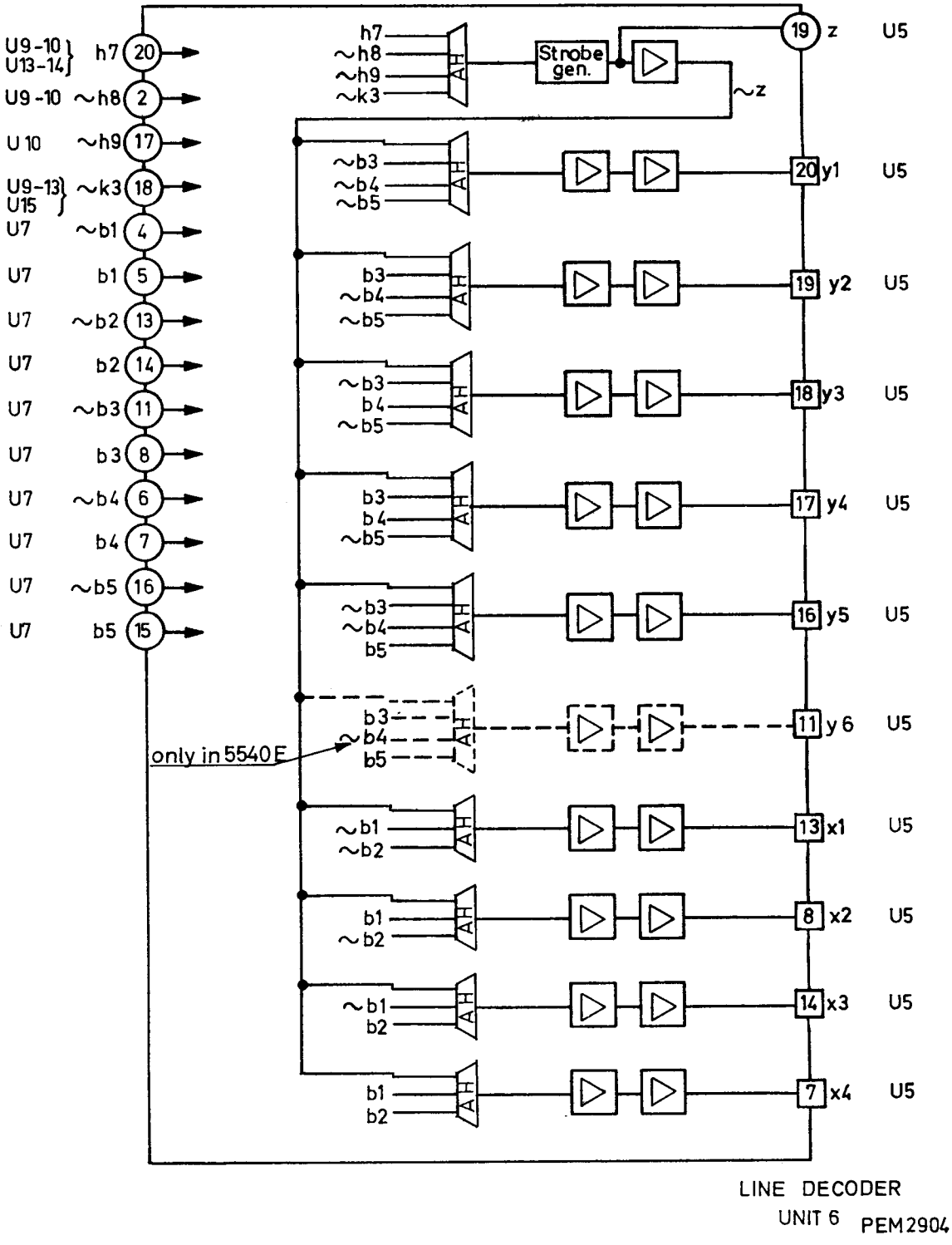
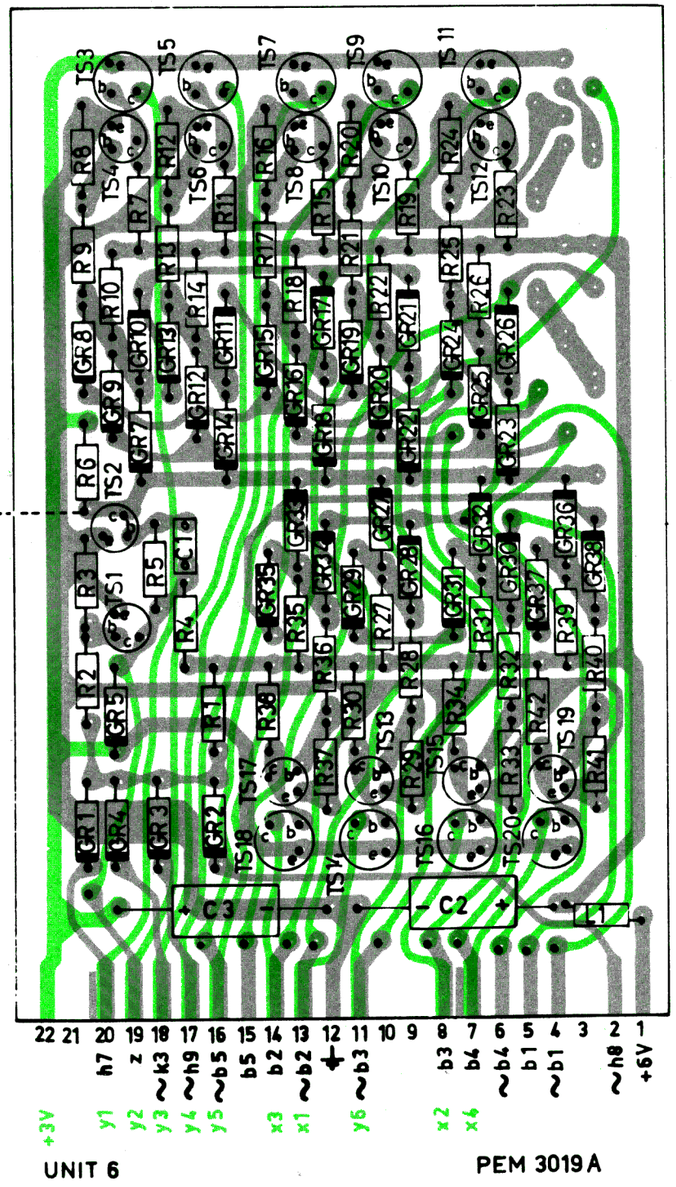


Fig. XII-3 Block-diagram, line decoder, Unit 6



XII-4a Printed wiring board, line decoder (A version), Unit 6

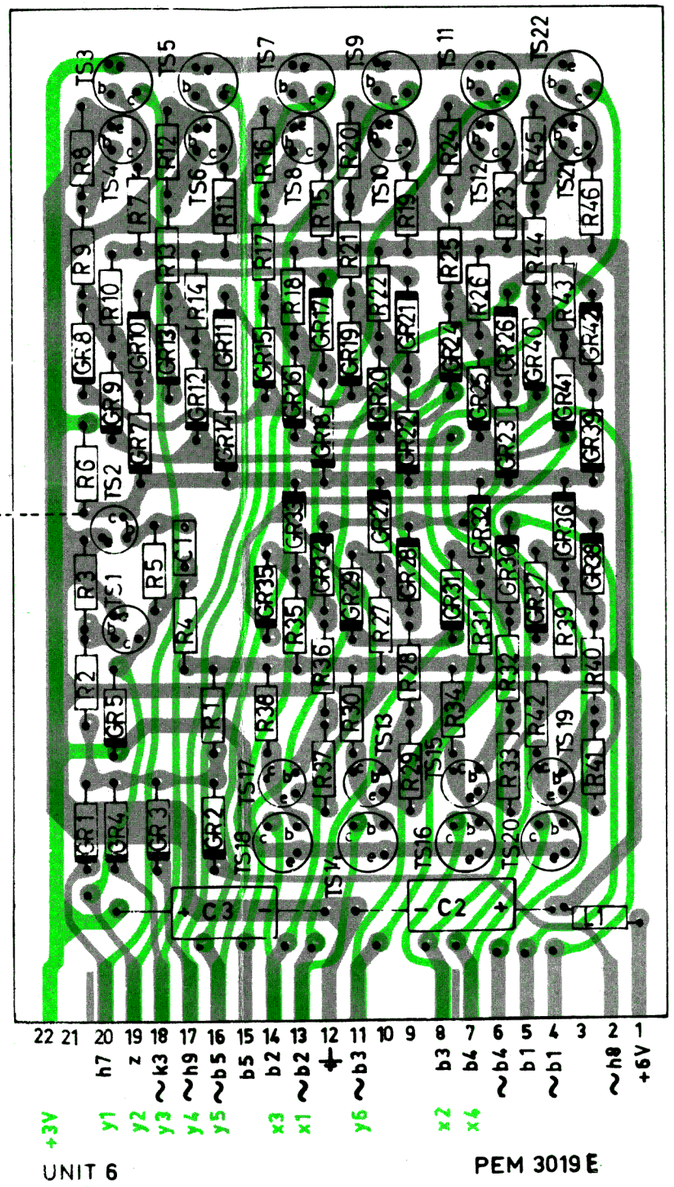


Fig. XII-4b Printed wiring board, line decoder (E version), Unit 6

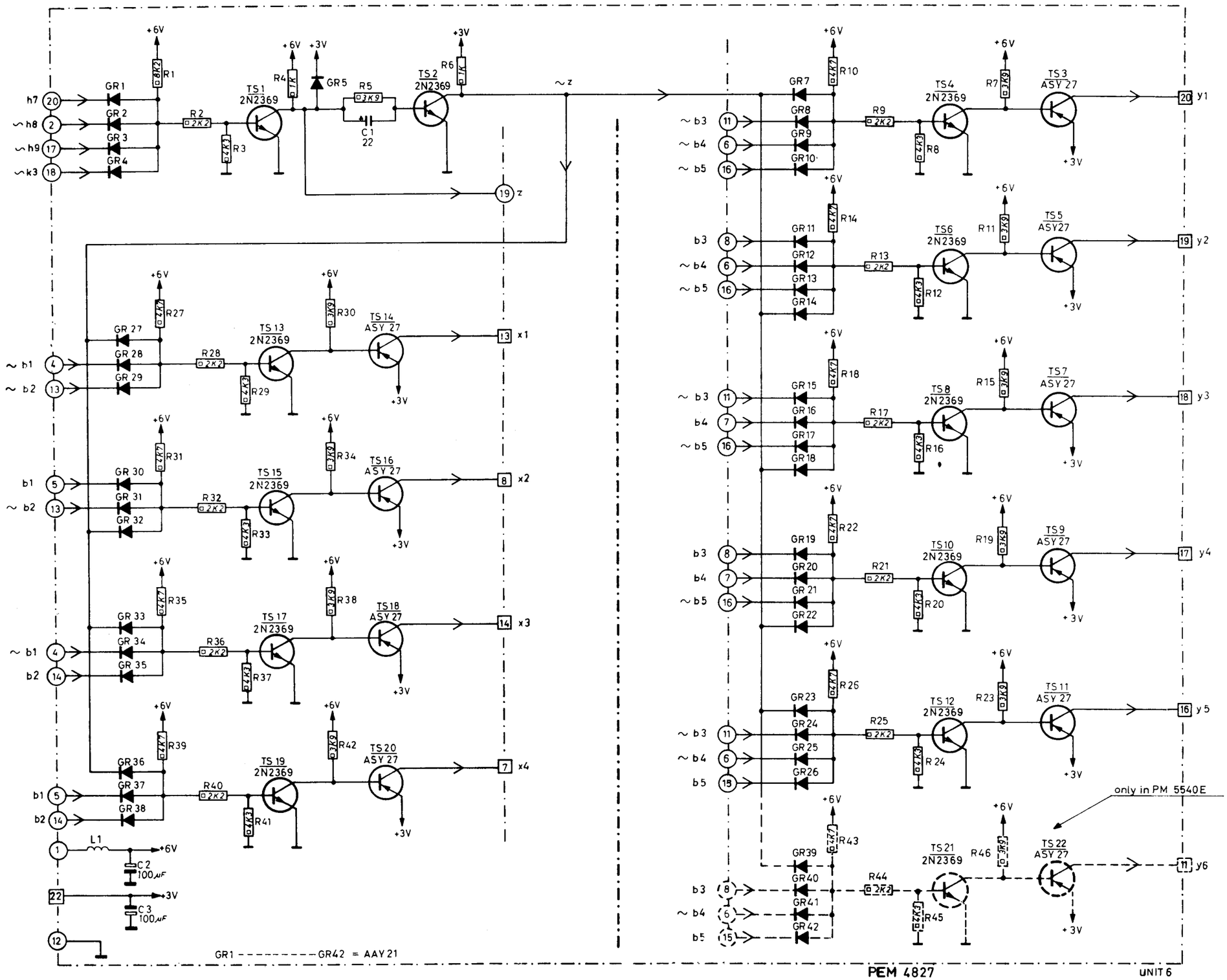


Fig. XII-5 Circuit diagram, line decoder, Unit 6

XIII Unit 7

The line-selector register

This register consists of the 5 cascade connected flip-flops CB1 . . . CB5, the AND-gates GR1 . . . GR3 and GR6 . . . GR8 succeeded respectively by the amplifiers TS1 and TS2.
The register can be set to zero (reset), set to 21[1]) (preset) and set to change over from forward to down-counting or vice versa.
The resetting is effected by the "k1" pulse combined with the "g2" and "∿ g4" pulses via GR1 . . . GR3 and TS1 to input 7 of CB1 . . . CB5. The setting to 21 is made by the "k1" pulse combined with the "g2" and "g4" pulses via GR6 . . . GR8 and TS2 to input 3 of CB1, CB3 and CB5.
The setting to forward- or down-counting is effected by the "∿ g4" and "g4" pulses respectively.

The functioning of the register is as follows.
During the last line of an interval in the upper half of the pattern, the register is set to zero. During each succeeding line the register counts forward the "∿ k1" pulses. After the register has counted to 21[1]), the last line of an interval is reached, and the reset will be made if the succeeding interval is still in the upper half of the pattern.
If the succeeding interval is in the lower half of the pattern, the register will be preset to 21[1]) instead of set to zero, and for each succeeding line the register will count down the "k1" pulses. At zero, presetting 21 will be read-in again, and the process will be repeated until the upper half of the next field occurs. Then the setting to zero with forward-counting will be arranged.
Pulses "∿ g4" and "g4" inform the register concerning the upper half or lower half respectively of the pattern.
Outputs "b1 . . . b5" and "∿ b1 . . . ∿ b5" of the register are supplied to the line decoder (unit 6) to give the 10 read-in pulses X1 . . . X4 and Y1 . . . Y6[2]).

[1]) For PM5540/A read 17

[2]) For PM5540/A read Y1 . . . Y5

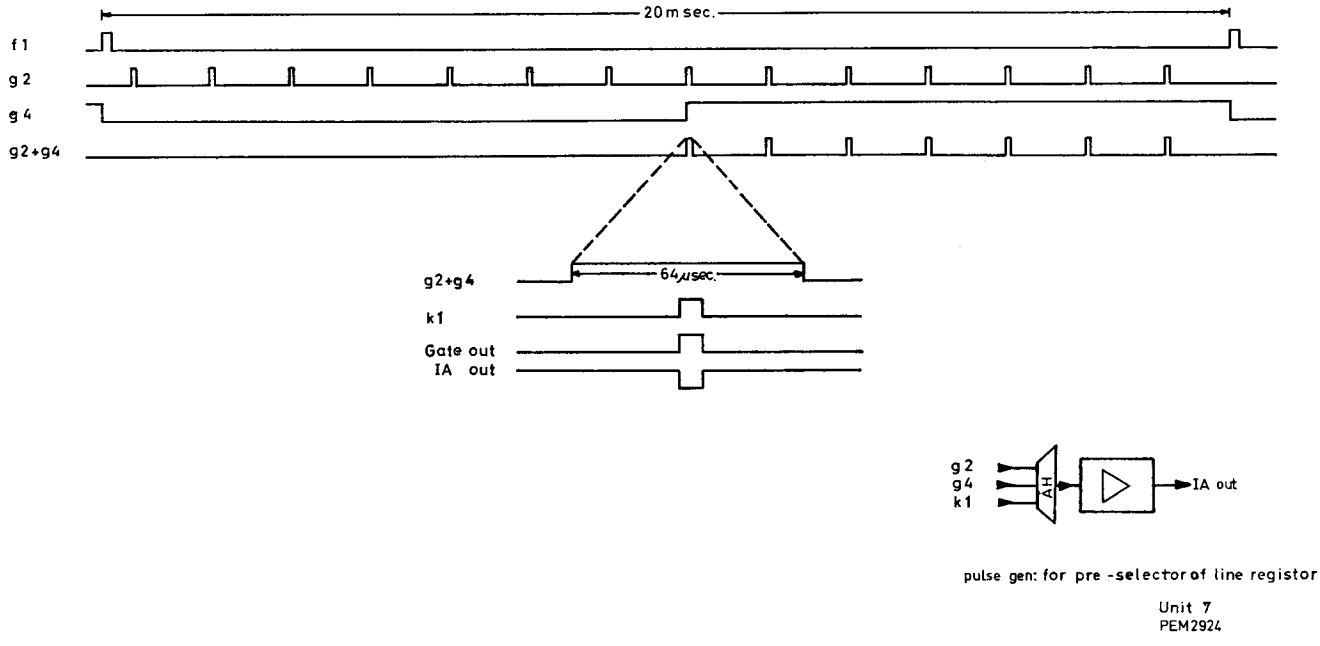


Fig. XIII-1 Pulse generator, pre-selector of line register

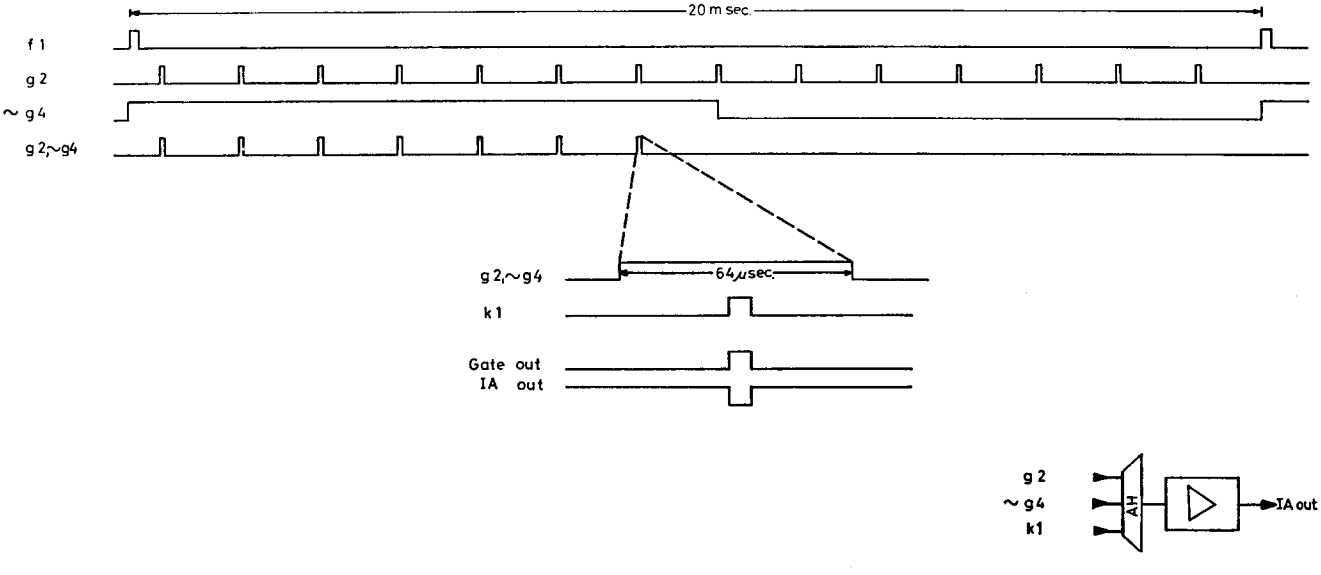


Fig. XIII-2 Pulse generator, pre-selector of line register

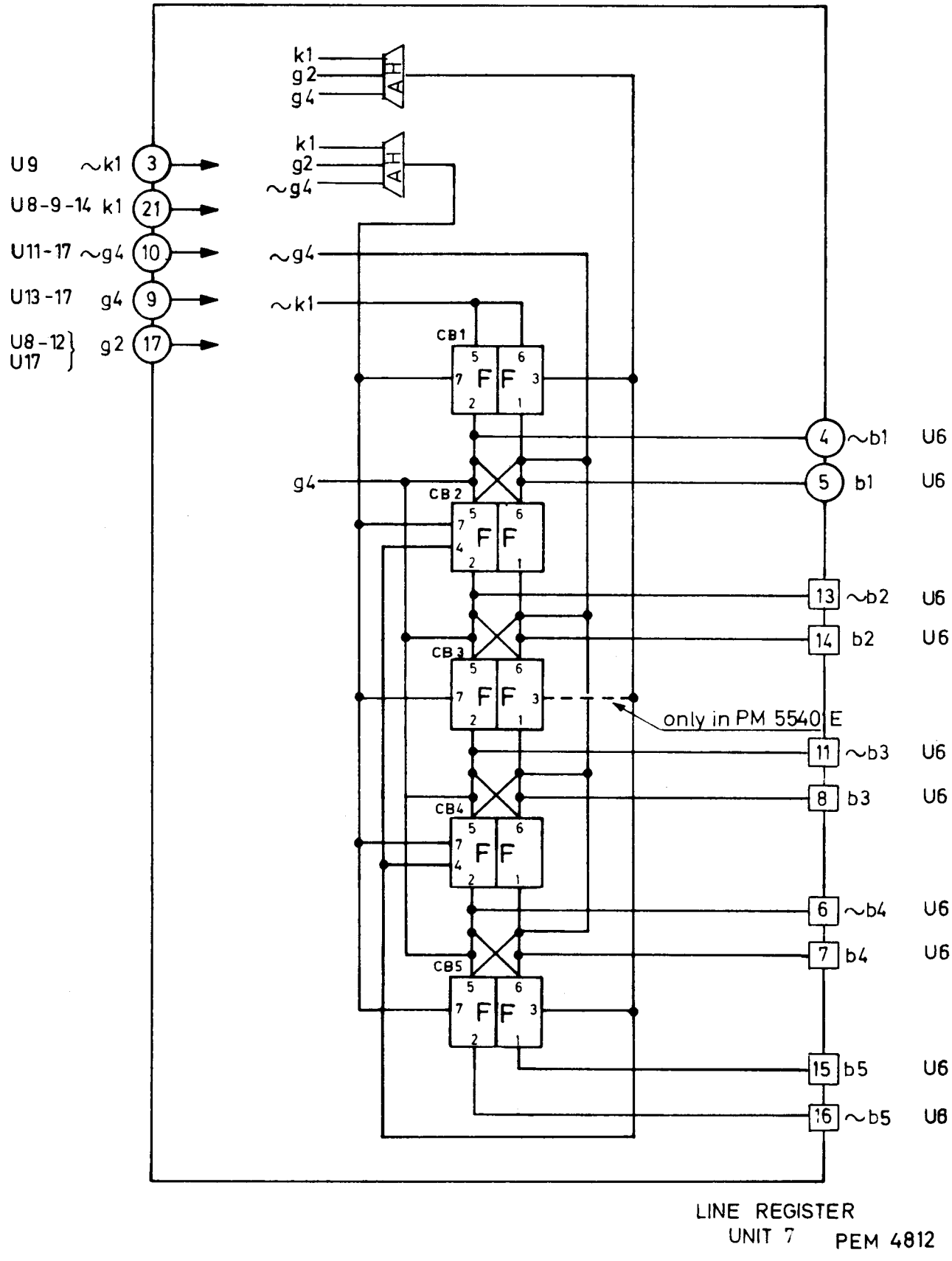


Fig. XIII-3 Block-diagram, line register, Unit 7

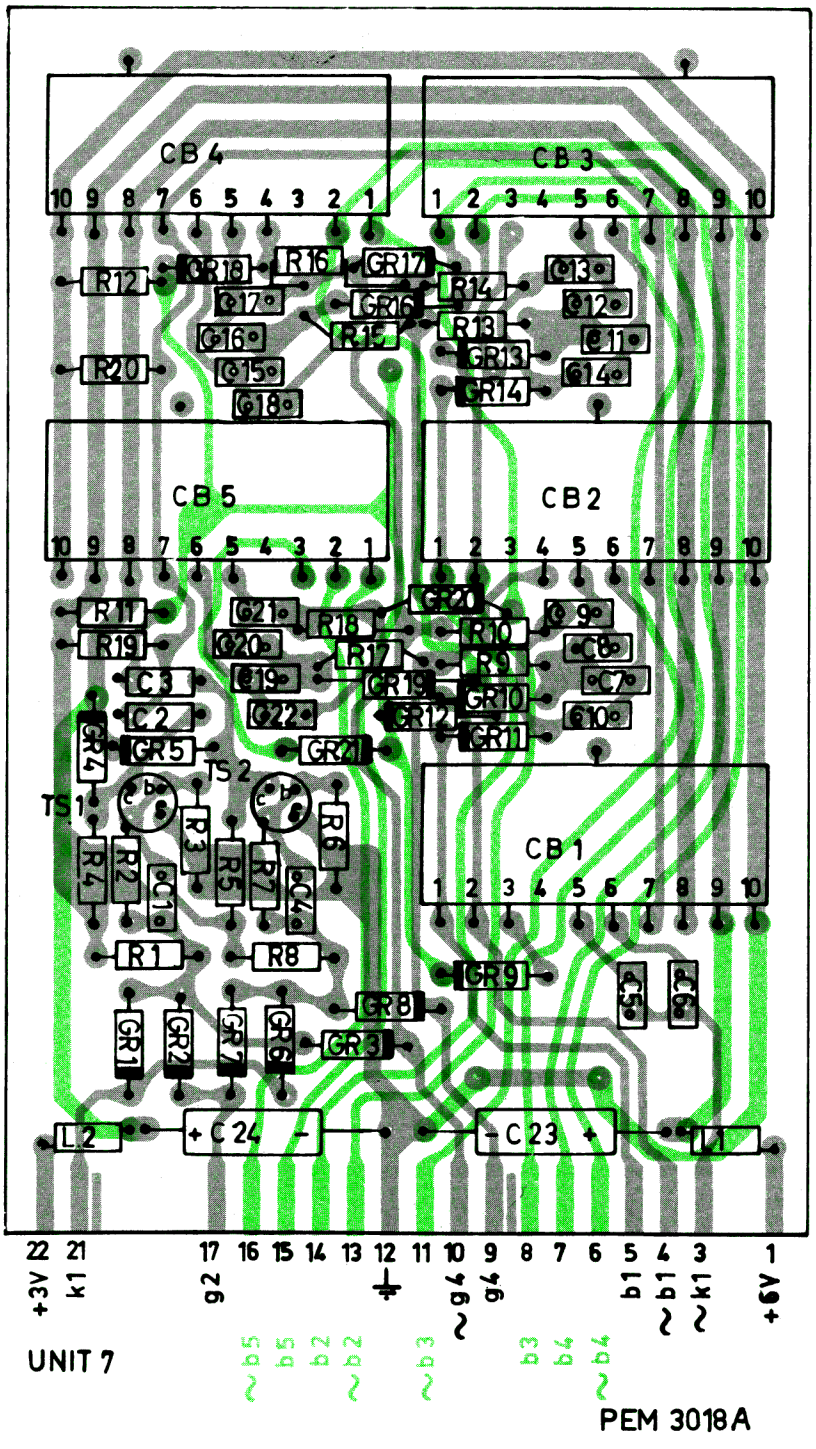


Fig. XIII-4a Printed wiring board, line register (A version), Unit 7

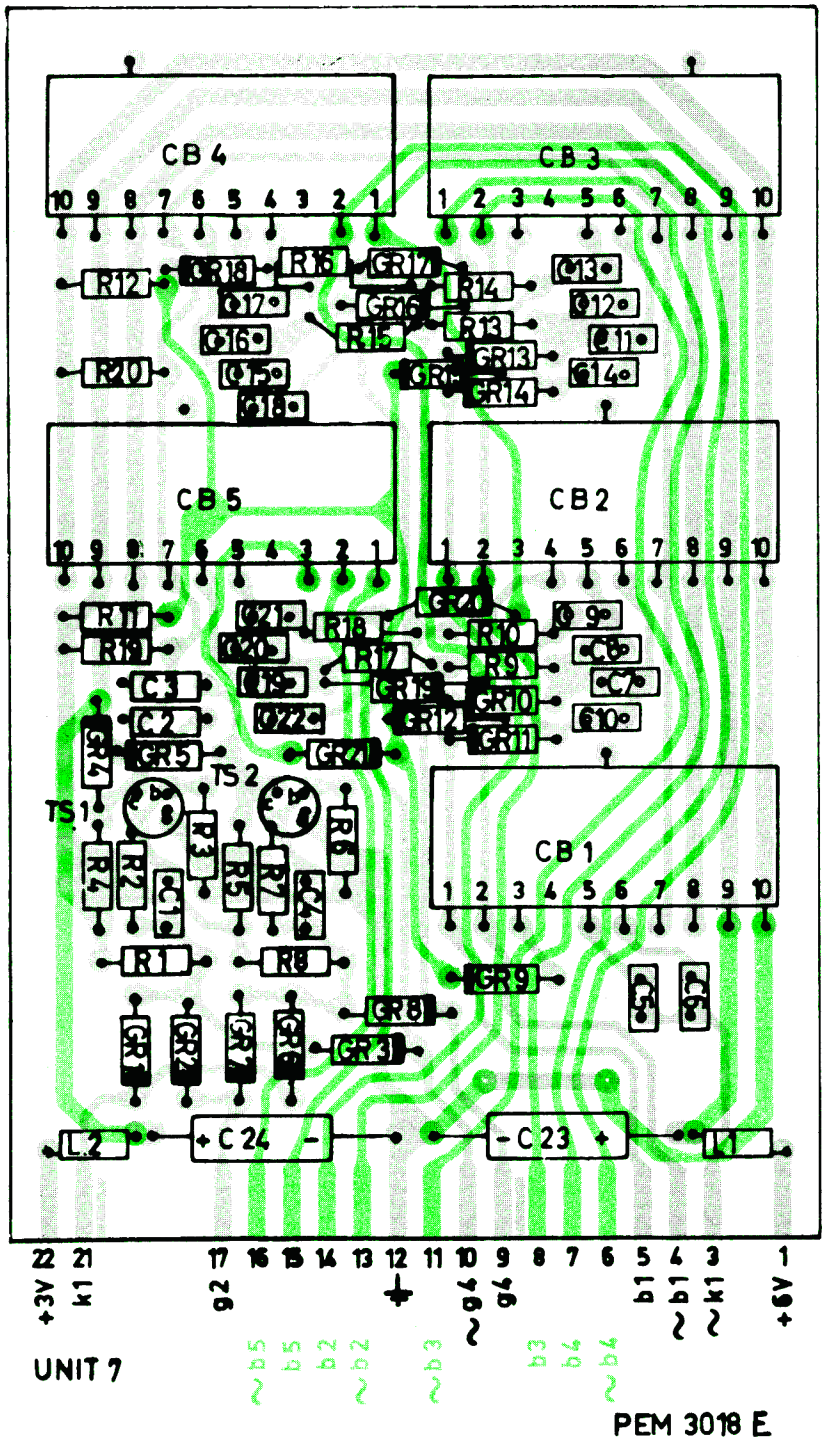


Fig. XIII-4b Printed wiring board, line register (E version), Unit 7

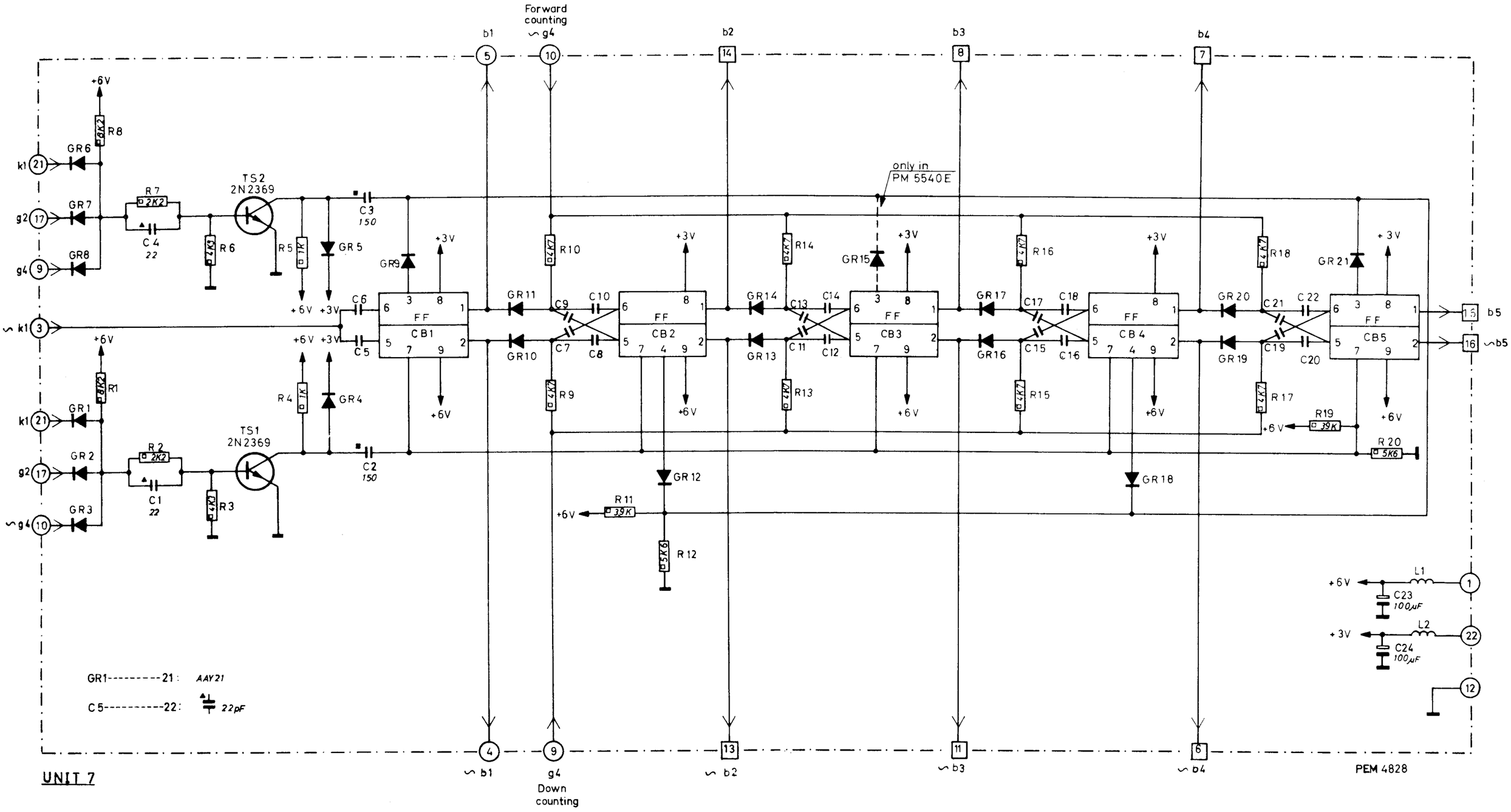
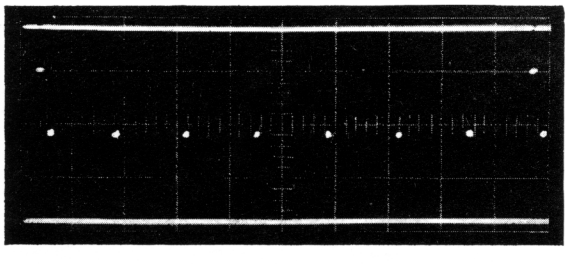


Fig. XIII-5 Circuit diagram, line register, Unit 7

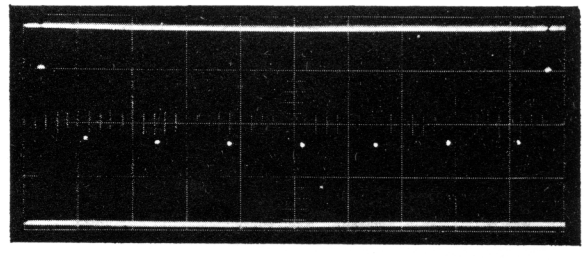
XIV Unit 8

The interval decoder

As mentioned in the description of the principle of the circle generator, the circle information will be deduced from seven different read-ins to the ferrite core memory.
The sequence of this information is determined by these read-in pulses. The pulses are supplied by the read-in amplifiers TS5 . . . TS18 and controlled by the AND- and OR-gates GR7 . . . GR26, GR28 . . . GR35 and GR37 . . . GR58. To simplify these gates, the following pulses are combined in the AND-gates GR1-GR3 and GR4 . . . GR6.
The "k1" pulse, controlling the moment and duration of the read-in (6 μs).
The "g2" pulse, opening the gate during the last line of the interval.
The "f8" and "∼ f8" pulses, producing the seven different intervals. The intervals number 5, 6 and 7 however, are used two times in one field.
The resulting pulses "q1" and "q2", are applied to the read-in gates.
The "g5" and "∼ g5" pulses are distinguishing between the two fields ("g5" for the first field and "∼ g5" for the second one).
The "∼ v7" pulse opens the gate withing the circle area.
The "v2" . . . "v6" pulses determine the moment at which the read-in concerned is made. The read-in currents, having a duration of 6 μs, are of a magnitude of 755 mA.



q1
2 V/cm 2 ms/cm
reference: frame sync.



q2
2 V/cm 2 ms/cm
reference: frame sync.

Fig. XIV-1 Oscilligrams, Unit 8

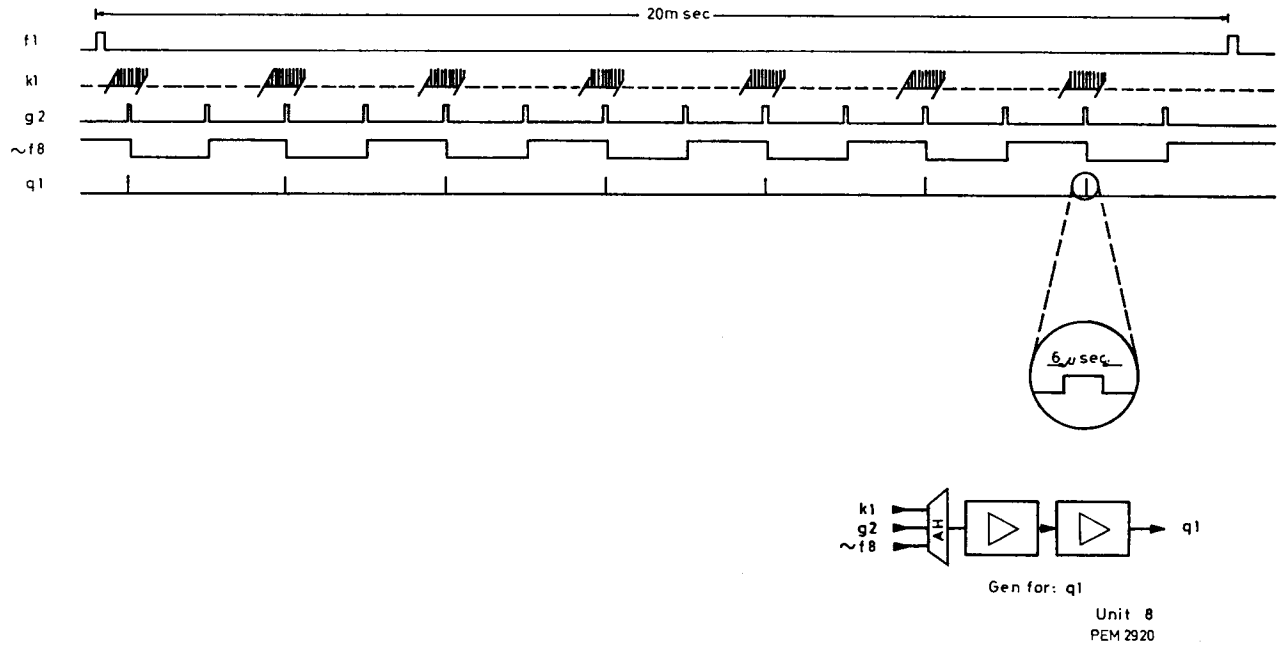


Fig. XIV-2 Pulse diagram for "q1"

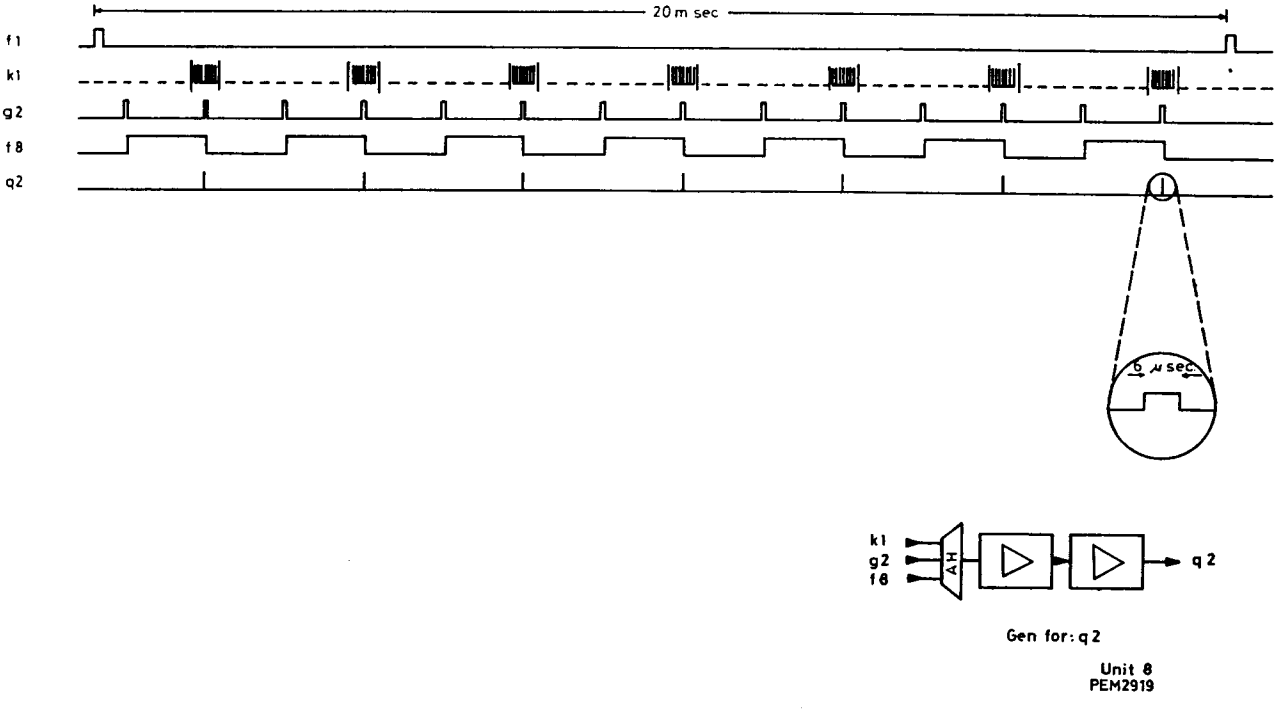


Fig. XIV-3 Pulse diagram for "q2"

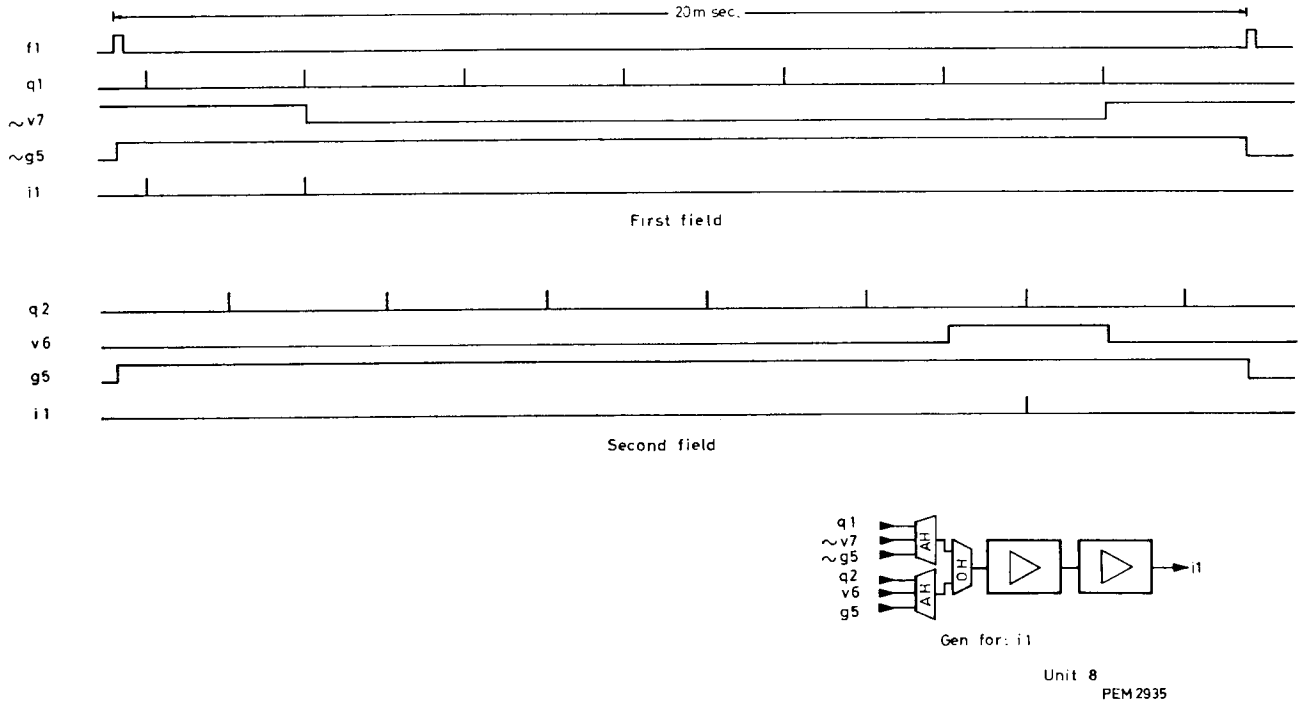


Fig. XIV-4 Pulse diagram for "i1"

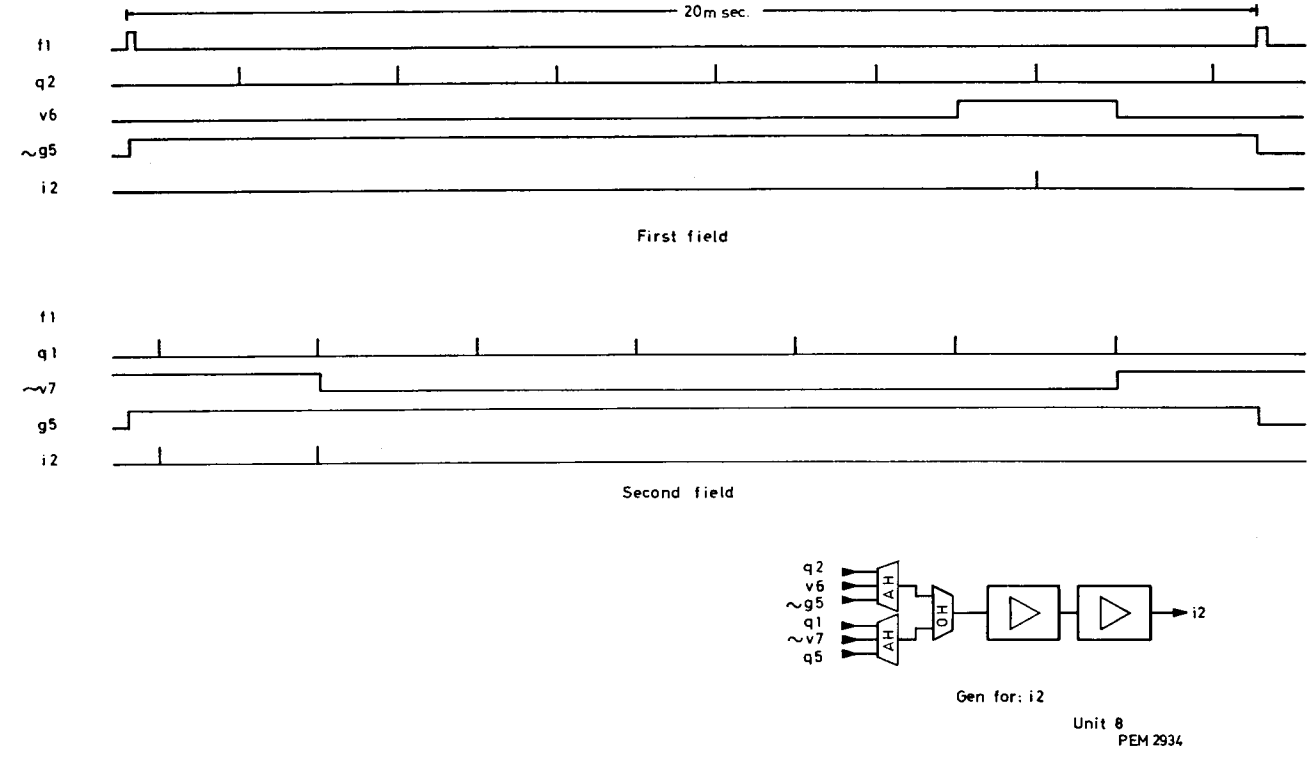


Fig. XIV-5 Pulse diagram for "i2"

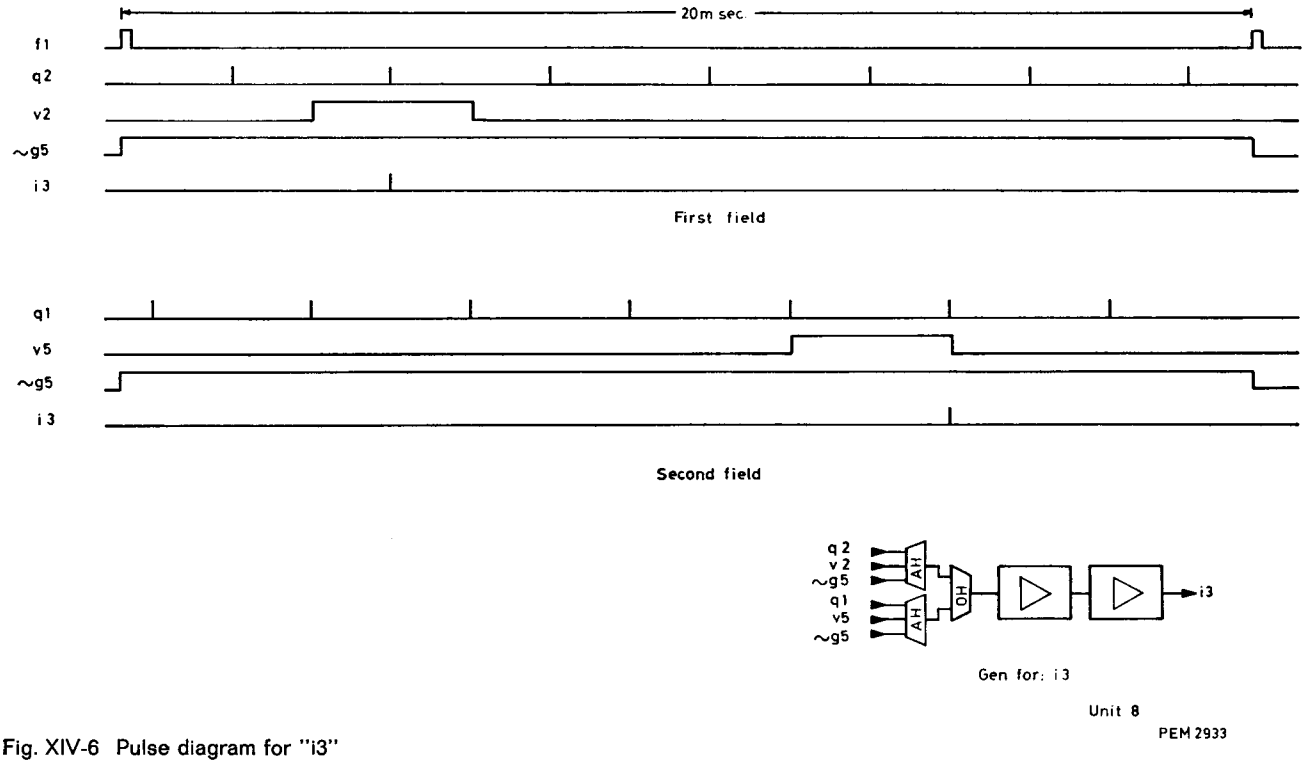


Fig. XIV-6 Pulse diagram for "i3"

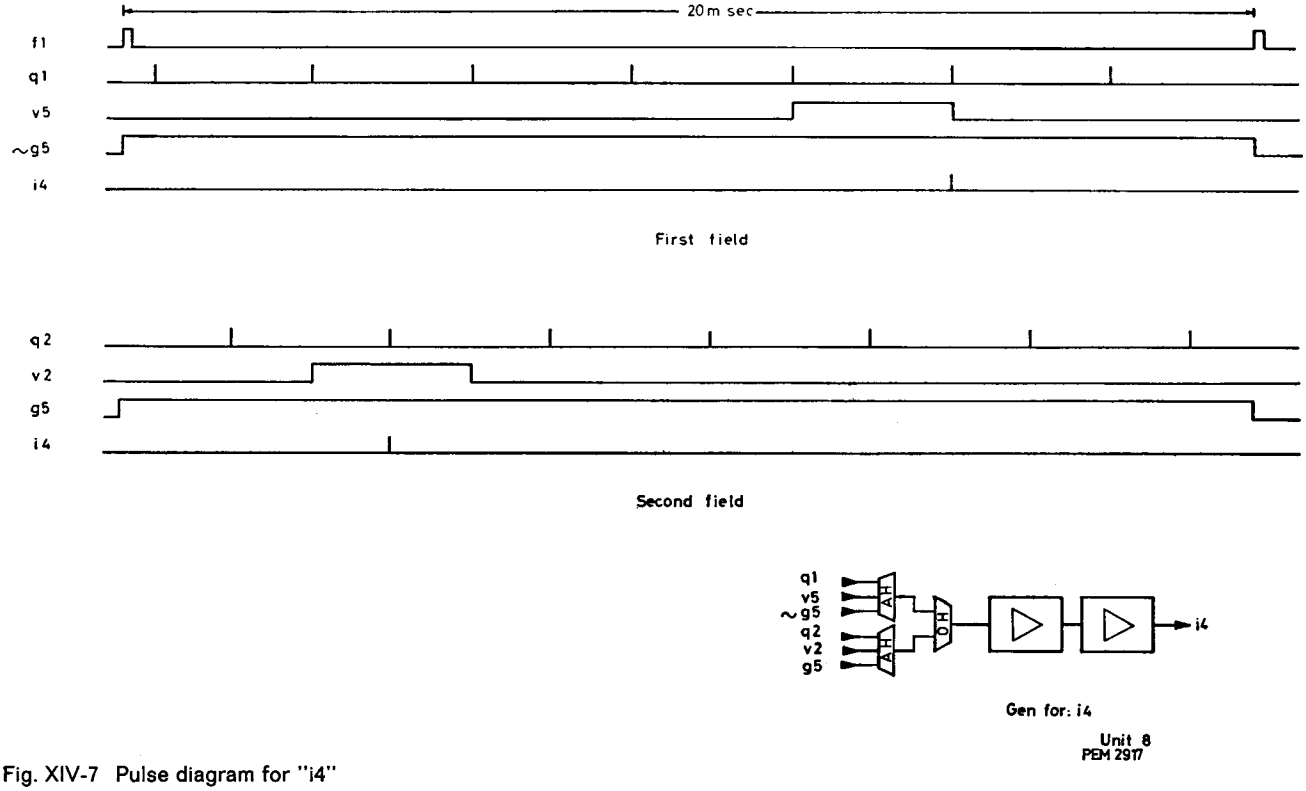


Fig. XIV-7 Pulse diagram for "i4"

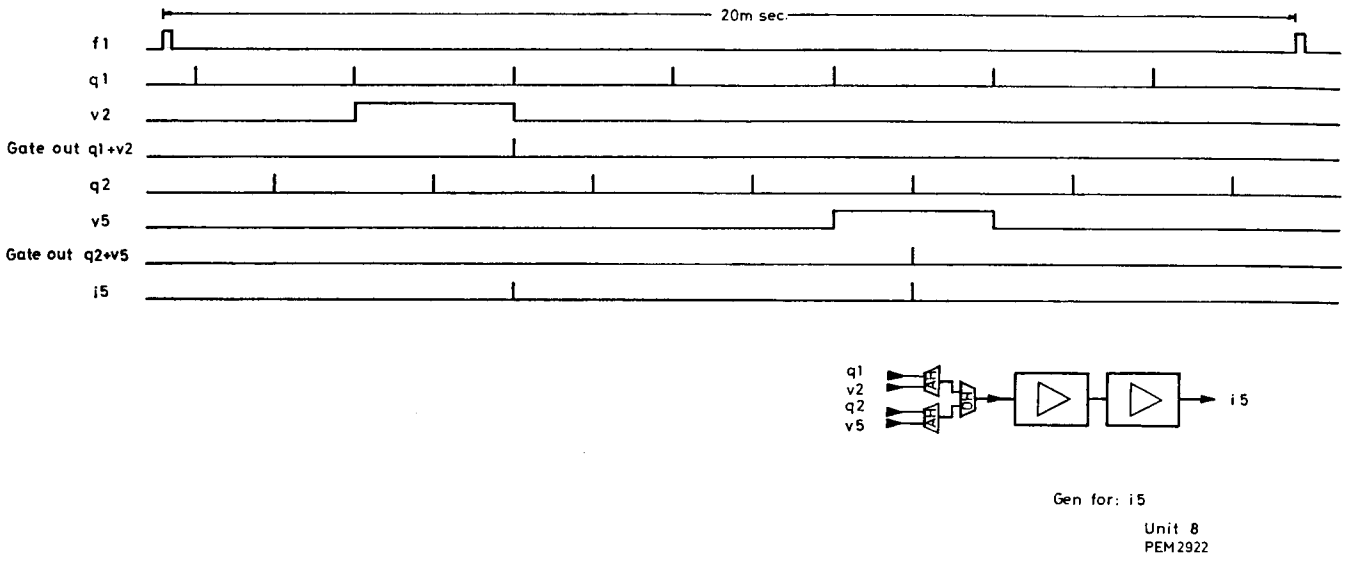


Fig. XIV-8 Pulse diagram for "i5"

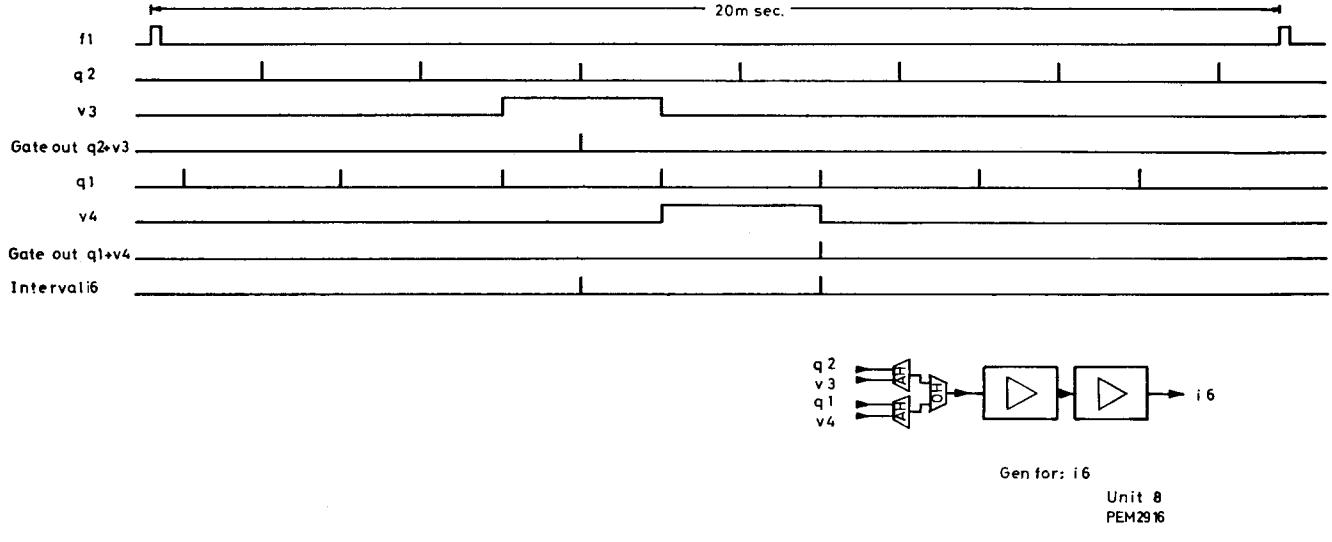


Fig. XIV-9 Pulse diagram for "i6"

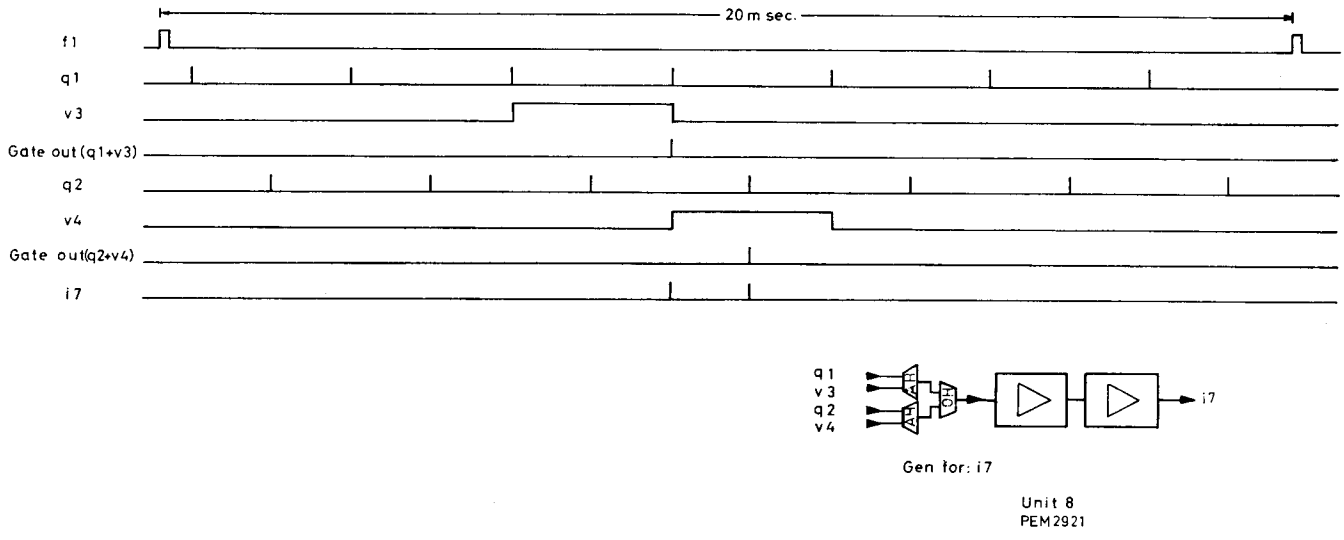


Fig. XIV-10 Pulse diagram for "i7"

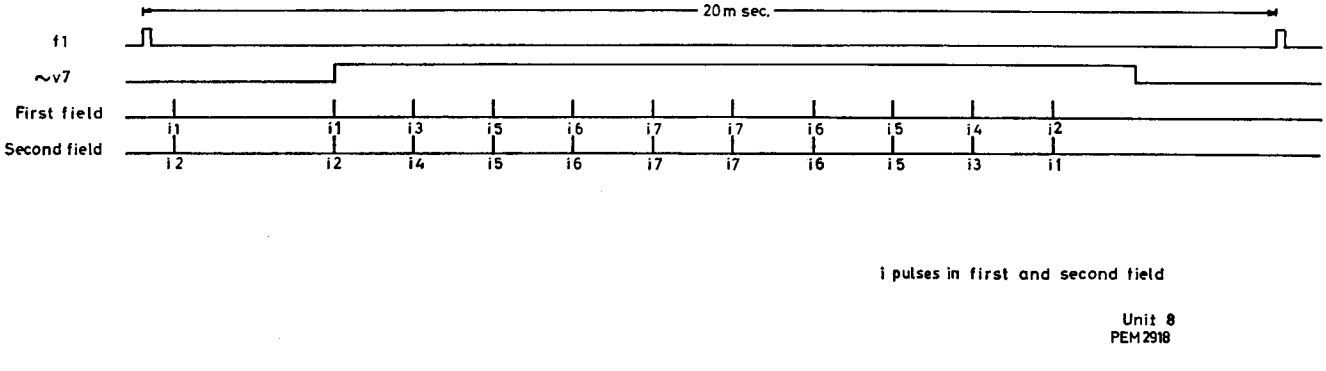


Fig. XIV-11 Arrangement of i-pulses

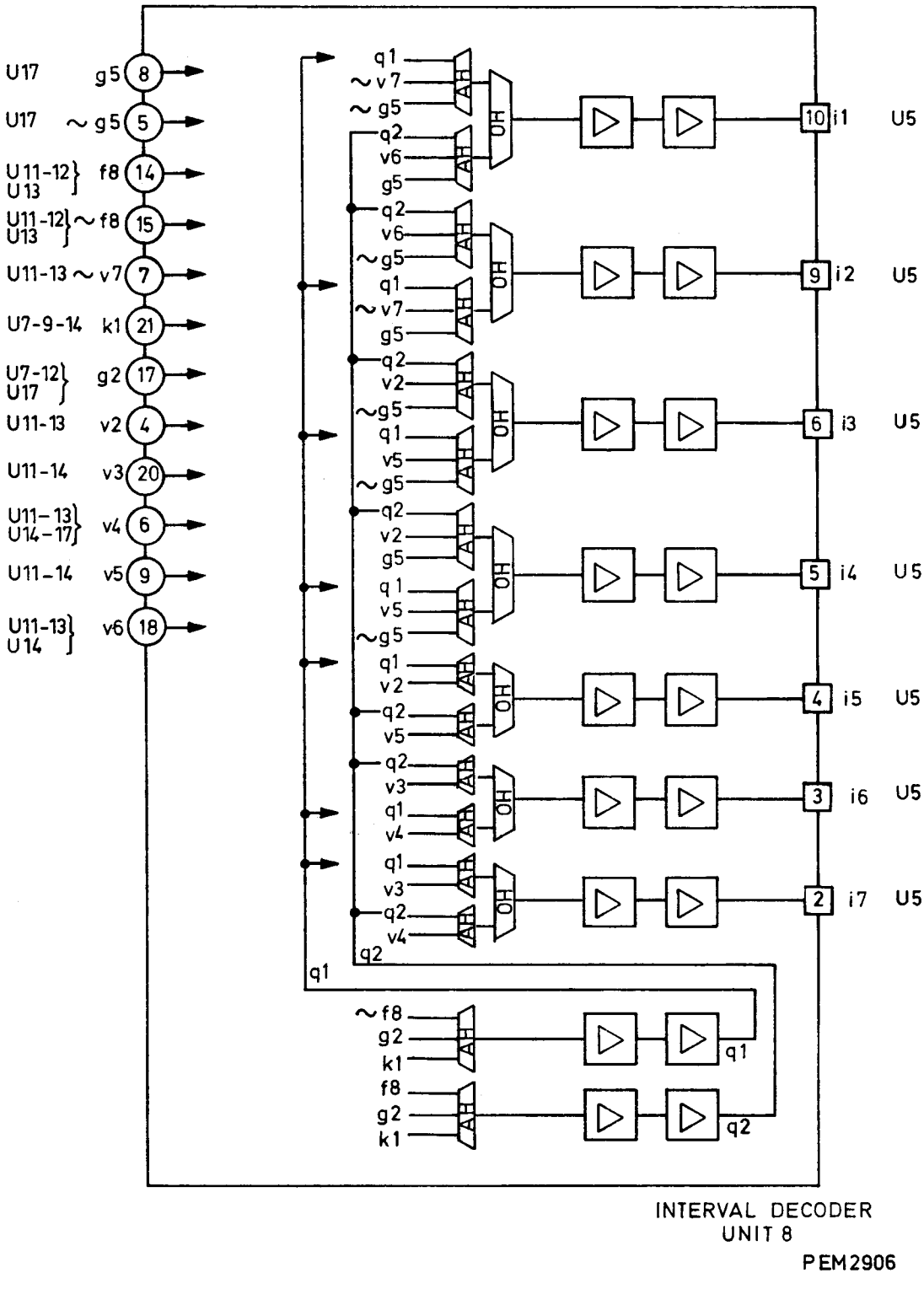


Fig. XIV-12 Block-diagram, interval decoder, Unit 8

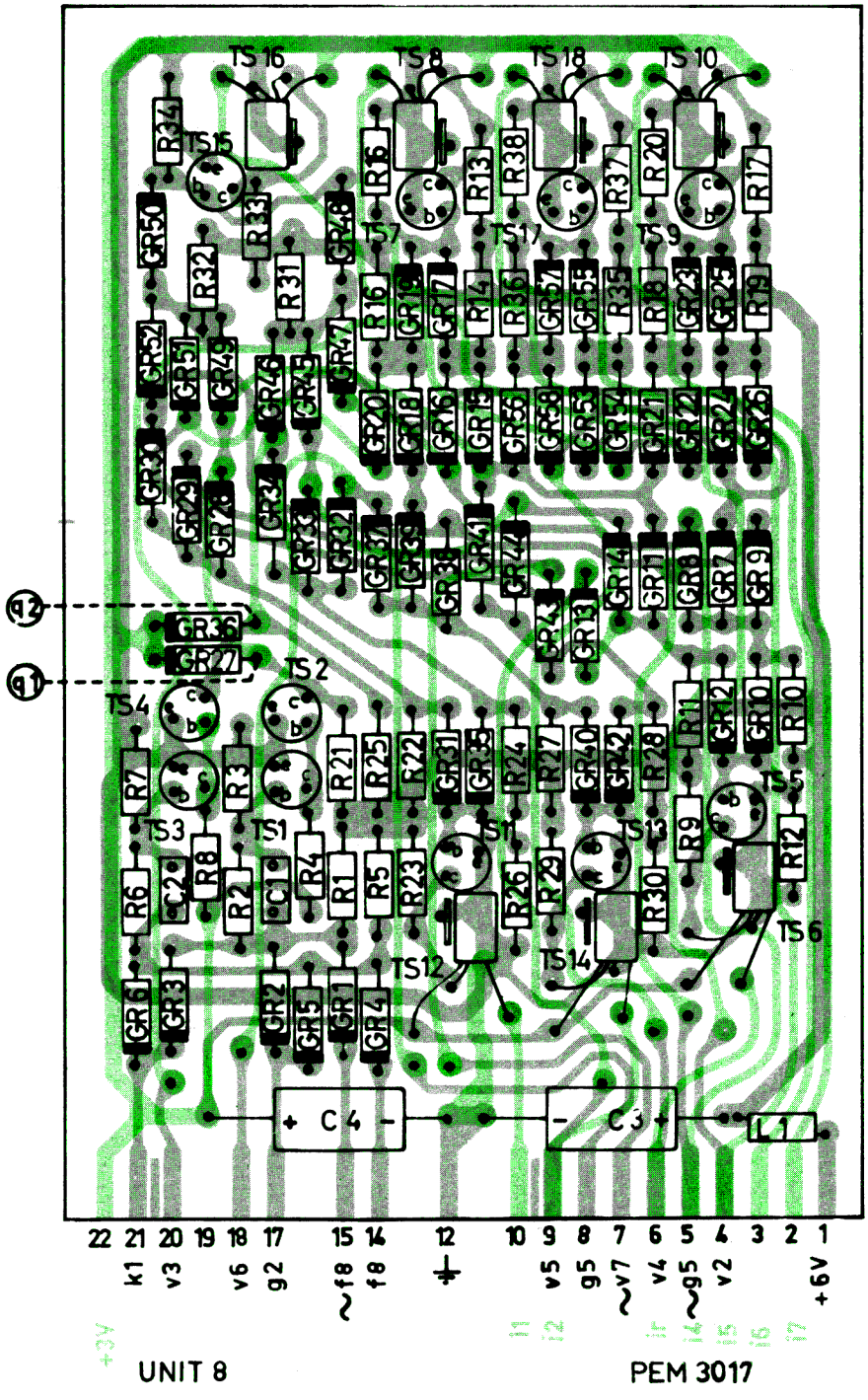
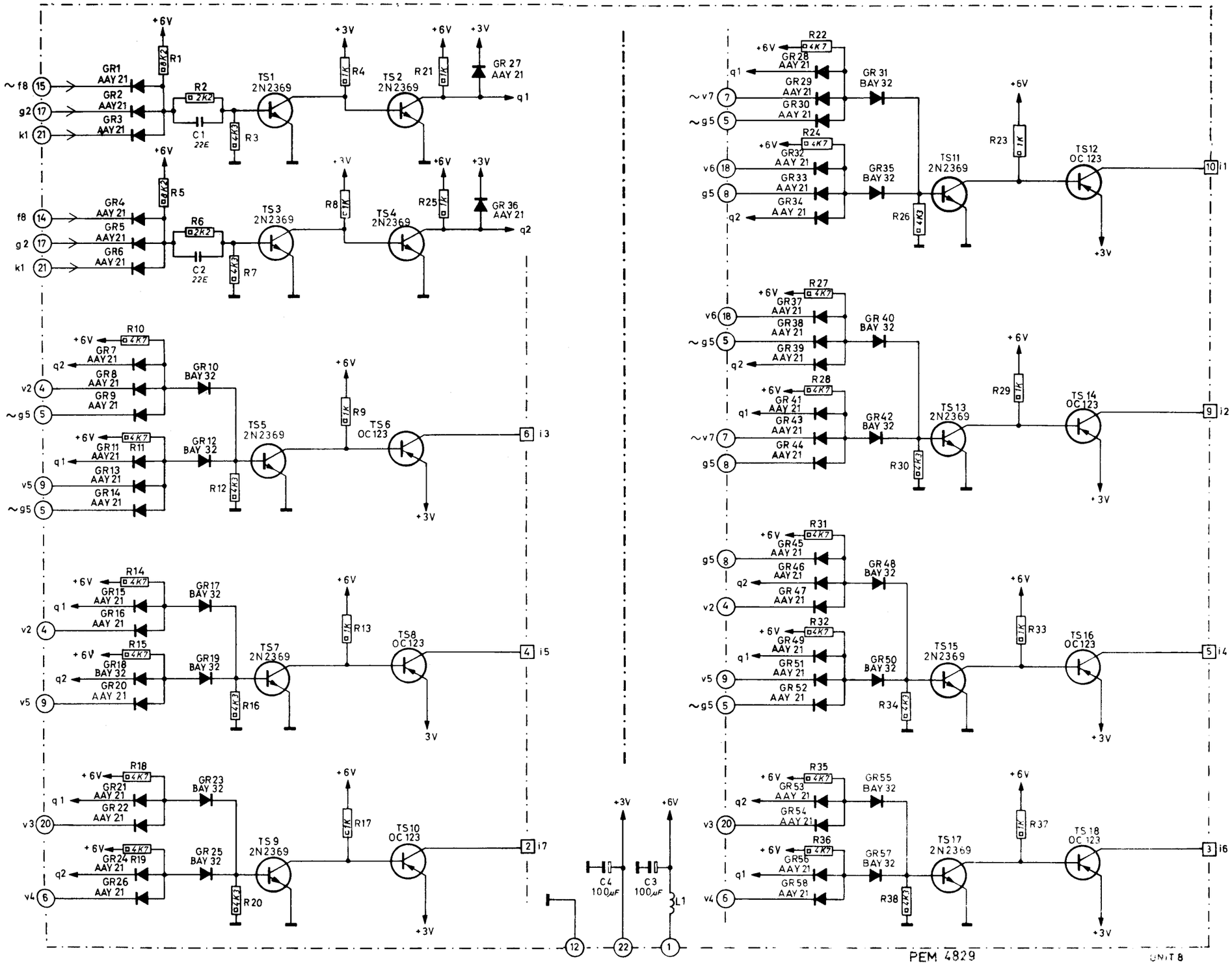


Fig. XIV-13 Printed wiring board, interval decoder, Unit 8



From version /06 TS8 - TS10 - TS12 - TS14 - TS16 and TS18 are of the type AC188 (4822 130 40456)

Fig. XIV-14 Circuit diagram, interval decoder, Unit 8

XV Unit 9

The horizontal decoder

The purpose of the decoder is to supply horizontal gating pulses. These pulses, based on pulses from the horizontal divider (unit 10), are produced by a group of generators.

Generator for the "k4" pulse
This generator consists of circuit block CB1 and the AND-gates GR1 . . . GR3 and GR4 . . . GR7.
In circumstances that the generator is not reset at the beginning of a line (eg. after switching) the "∿ h1" pulse ensures that this will be done.
The generated "k4" and "∿ k4" pulses are applied to the cross-bare gate (unit 15) where they determine the vertical borders of the crossed lines pattern (see Fig. XXII-1).

Generator for the "k3" pulse
This generator consists of CB2 and GR8 . . . GR10 and is set to zero for each line by the "∿ h1" pulse; it is controlled by the "h3", "h5" and "k1" pulses.
The generated pulse "k3" is applied to unit 13 and the "∿ k3" pulse to the units 6, 13 and 15.
These pulses produce the black/white steps in the top and bottom-segments of the circle (see Fig. XXII-1).

Generator for the "k2" pulse
This generator consists of CB3 and the two AND-gates GR23, GR24 and GR25 . . . GR29.
The generated pulse "∿ k2" is applied to unit 13 and produces the wide black bar in the black/white steps pattern.

Generator for the "k1" pulse
This generator consists of AND-gate GR11 . . . GR13, amplifiers TS1 . . . TS2, and clampers GR14 and GR15. It is controlled by the "h7", "∿ h8" and "k2" pulses.
TS2 is operating as an inverter while GR14 . . . GR15 clamp the "k1" and "∿k1" pulses to +3 V. The "∿ k1" pulse is applied to unit 7, the "k1" pulse to units 7, 8 and 14.
In the last unit, the "k1" pulse helps producing the horizontal staircase signal as well as the definition lines in horizontal sequence.

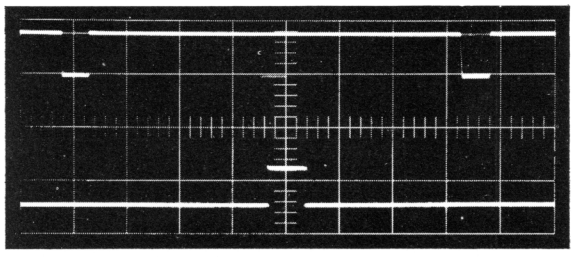
Generator for the "k5" pulse
This generator, consisting of the AND-gates GR16 . . . GR19, the OR-gate GR20 . . . GR22 and the amplifiers TS3 . . . TS5, is controlled by the "h1", "h8", "∿ k3", "k4" and "∿ k4" pulses. The pulses produced by the AND-gates are directed, via the OR-gate, to the amplifiers.
The generated pulses "k5" and "∿ k5" are applied to units 3 and 4 and control the forward or- down-counting of the circle register.

Generator for the "k6" pulse
This generator, consisting of AND-gate GR34-GR35 and amplifier TS6, is controlled by the "k2" and "v7" pulses. The generated pulse "∿ k6" is applied to unit 4 and determines "Start" of the clock-oscillator.

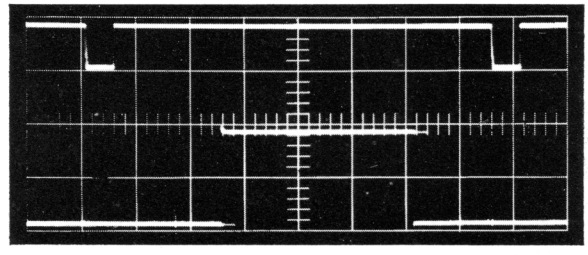
Generator for the "k7" pulse
This generator consisting of AND-gate GR30 . . . GR33, is controlled by the "h2", "h5", "∿ h6" and "k1" pulses. The generated pulse "k7" is applied to unit 4 and determines "Stop" of the clock oscillator during reversal of the counting sense of the circle register (unit 3) in the middle of a line.

Generator for the "h3" pulse
This generator (a one-shot multivibrator) consisting of GR36, TS7 and TS8. is controlled by the "h2" pulse. The generated pulse "h3", is applied to the generators producing the "k2" and "k3" pulses.

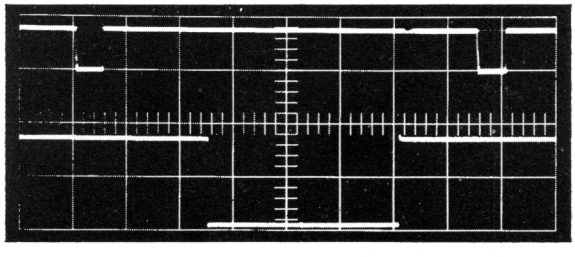
For checking and adjusting, see chapter X, units 3 and 4.



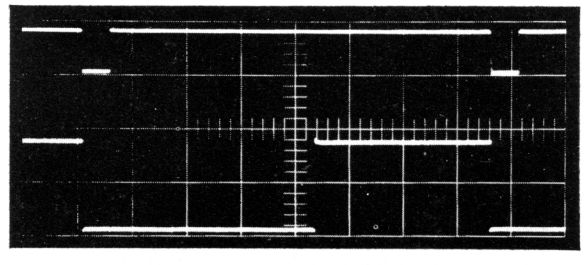
k1
5 V/cm 8 µs/cm
reference: line sync.



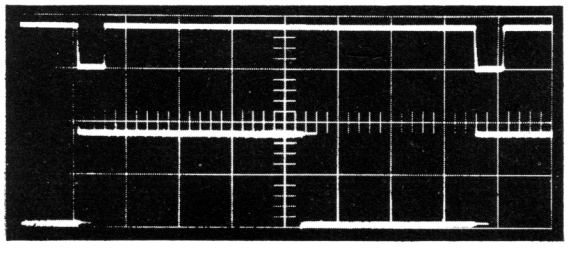
k2
2 V/cm 8 µs/cm
reference: line sync.



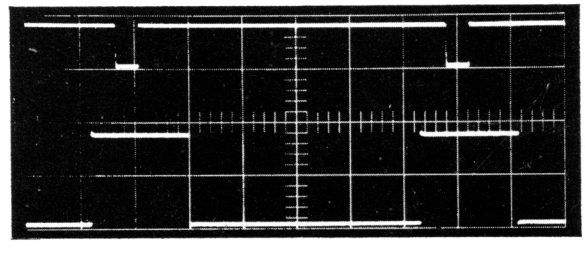
~ k2
2 V/cm 8 µs/cm
reference: line sync.



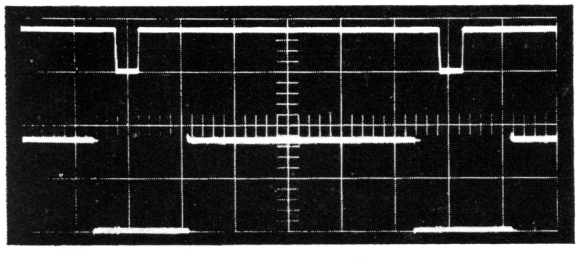
k3
2 V/cm 8 µs/cm
reference: line sync.



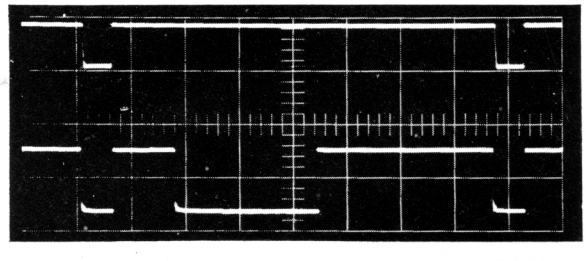
~ k3
2 V/cm 8 µs/cm
reference: line sync.



k4
2 V/cm 10 µs/cm
reference: line sync.

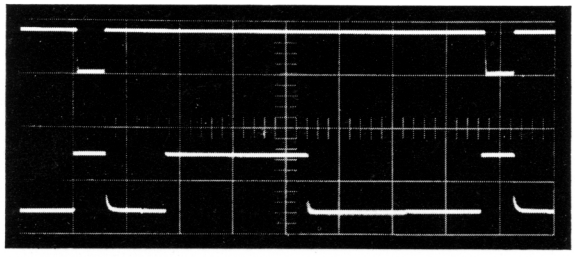


~ k4
2 V/cm 10 µs/cm
reference: line sync.

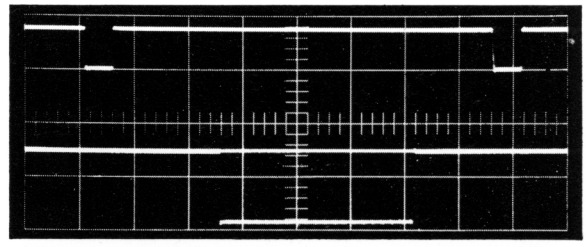


k5
5 V/cm 8 µs/cm
reference: line sync.

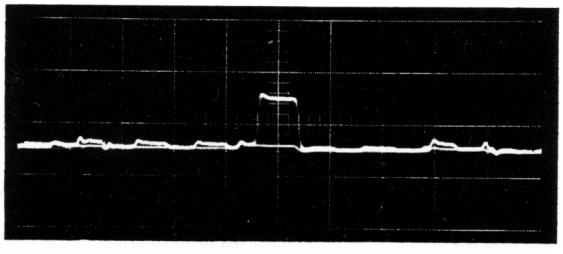
Fig. XV-1 Oscillograms, Unit 9



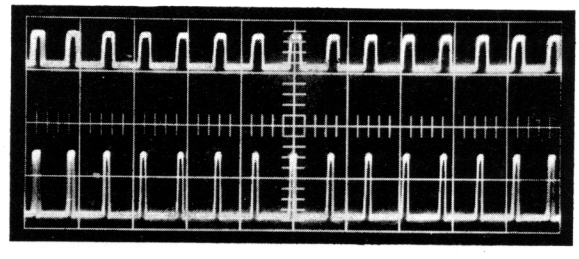
~ k5
5 V/cm 8 µs/cm
reference: line sync.



~ k6
1 V/cm 8 µs/cm
reference: line sync.



k7
1 V/cm 400 ns/cm



h3
5 V/cm 2 µs/cm
reference: h2 pulse

Fig. XV-1 Oscillograms, Unit 9

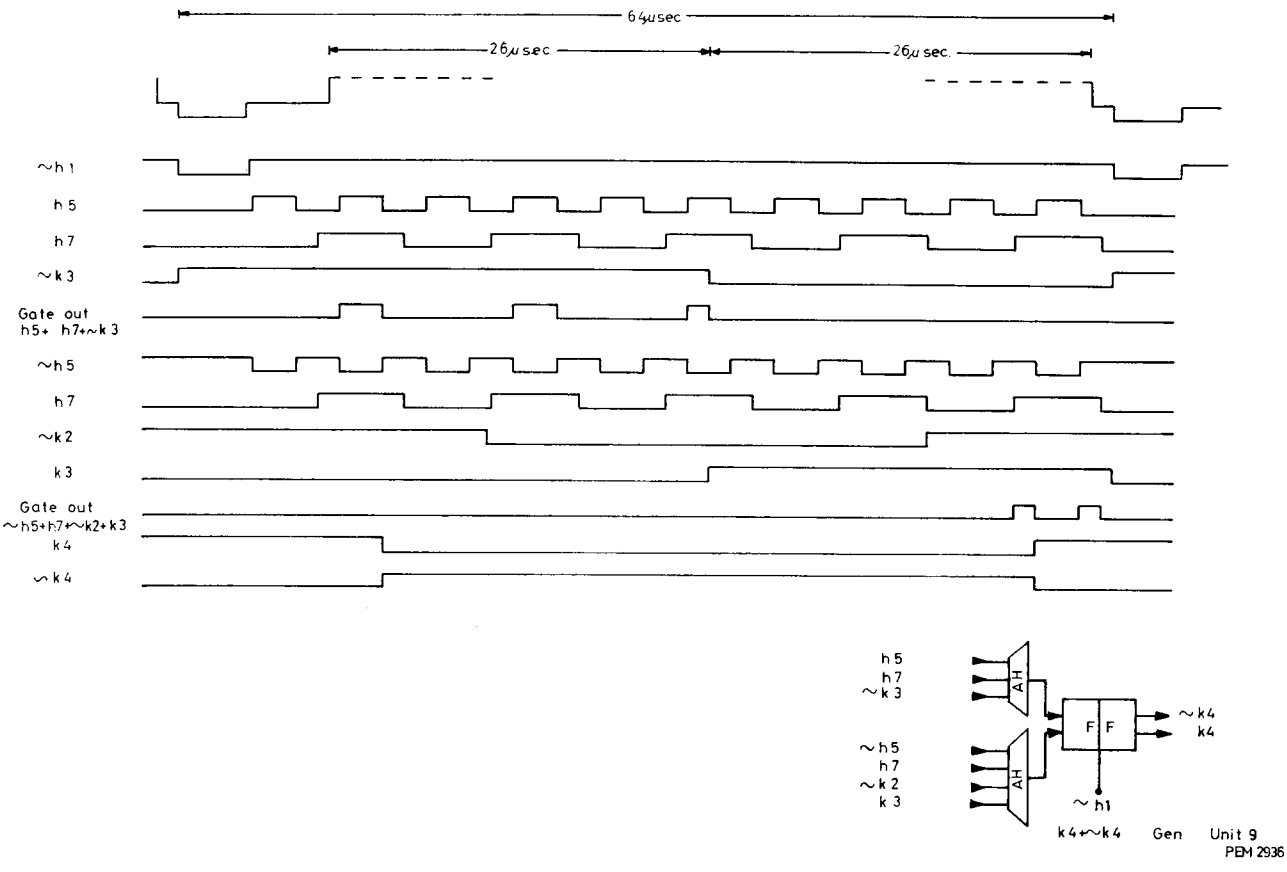


Fig. XV-2 Pulse diagrams for "k4" and "~ k4"

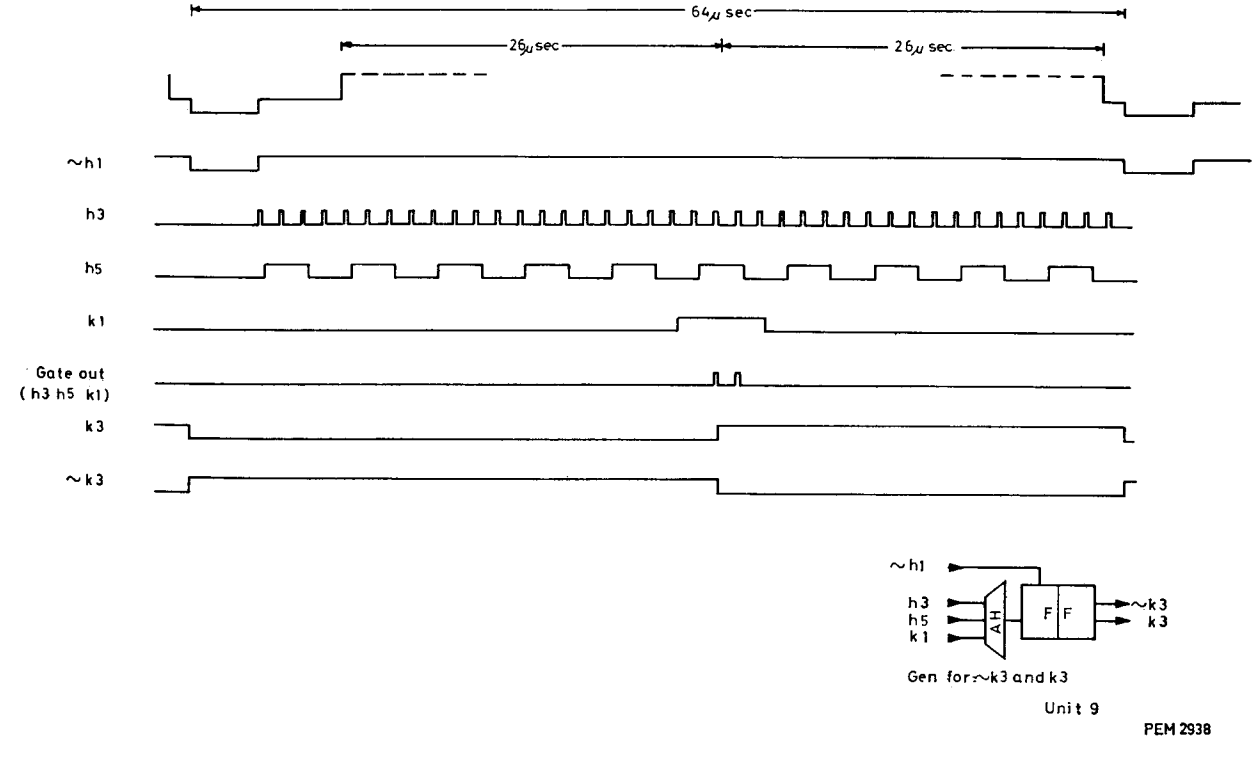


Fig. XV-3 Pulse diagrams for "k3" and "~ k3"

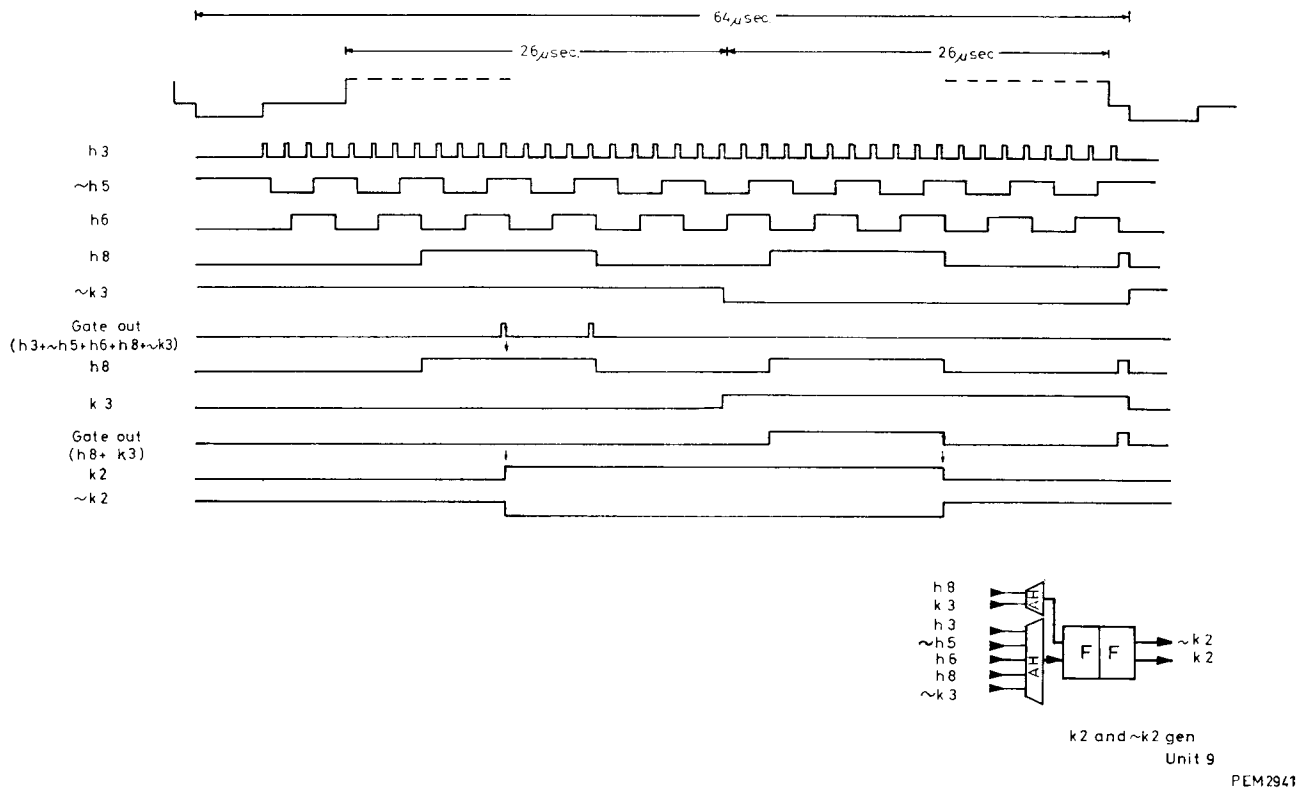


Fig. XV-4 Pulse diagrams for "k2" and "~ k2"

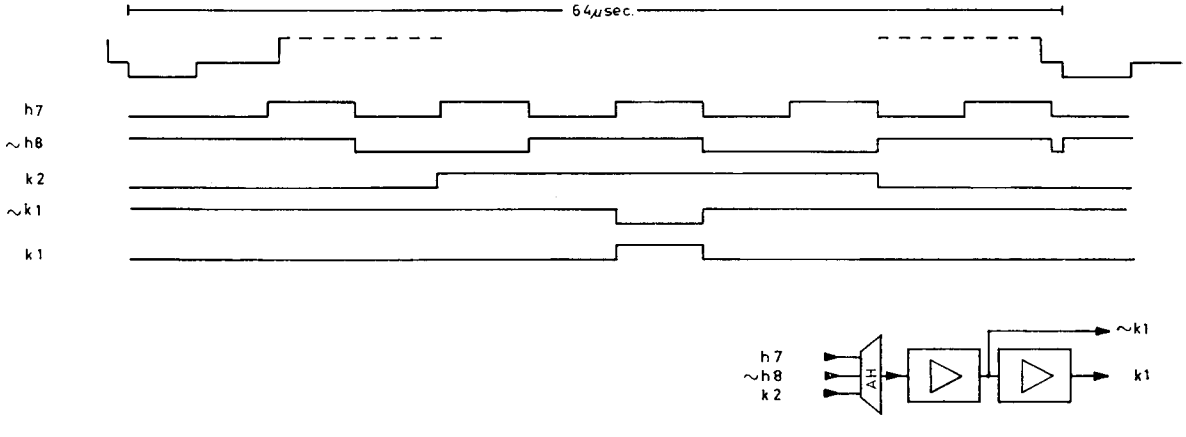


Fig. XV-5 Pulse diagrams for "k1" and "~ k1"

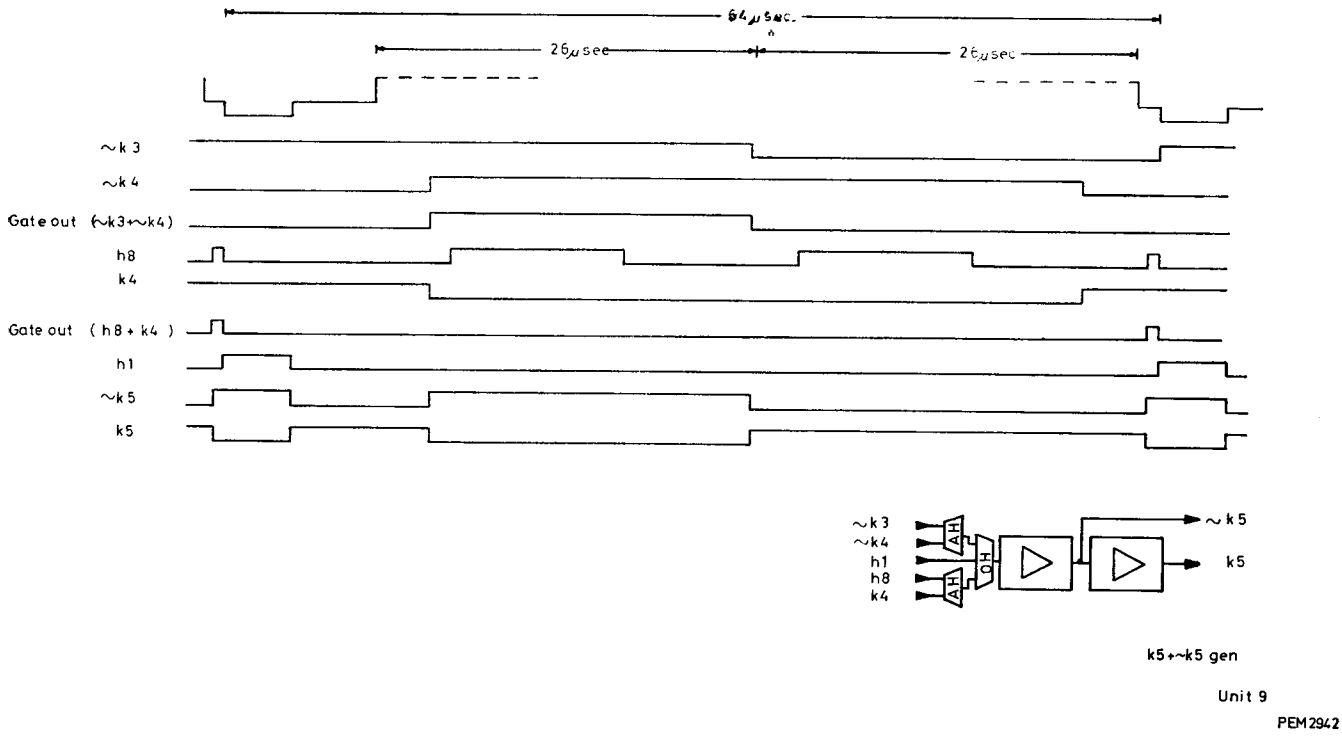


Fig. XV-6 Pulse diagrams for "k5" and "~ k5"

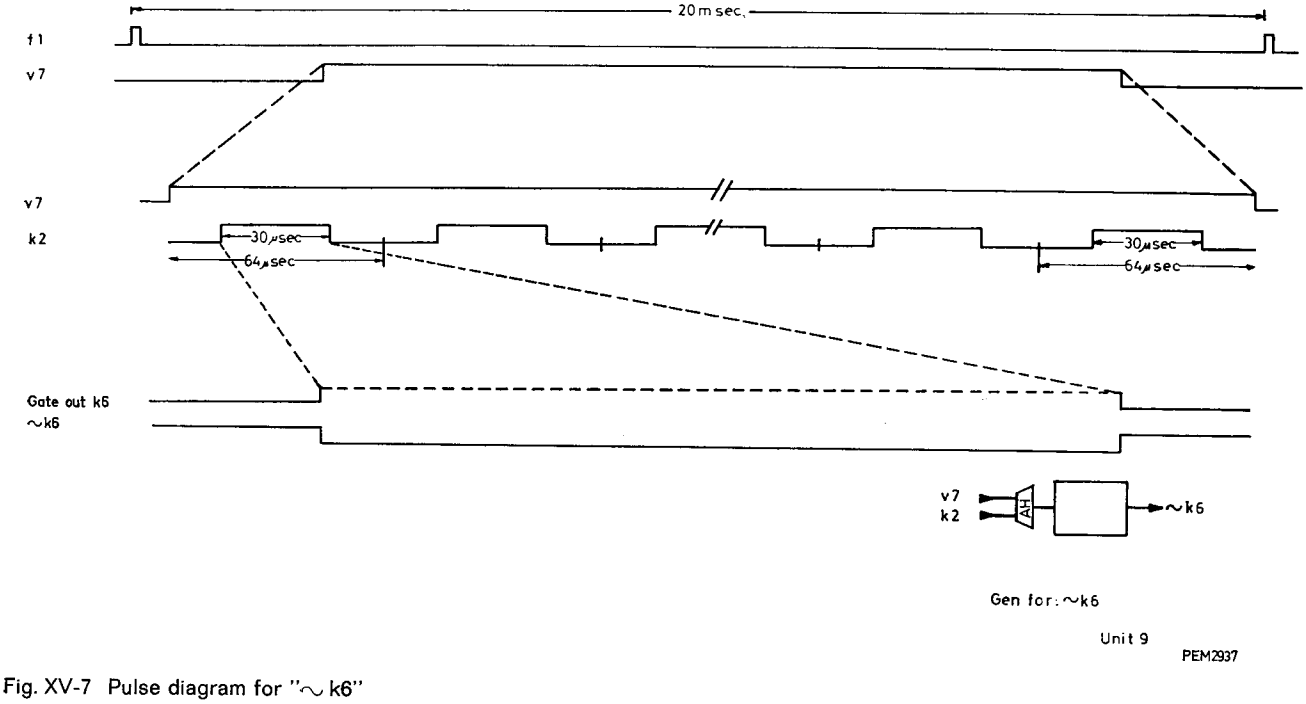


Fig. XV-7 Pulse diagram for "~ k6"

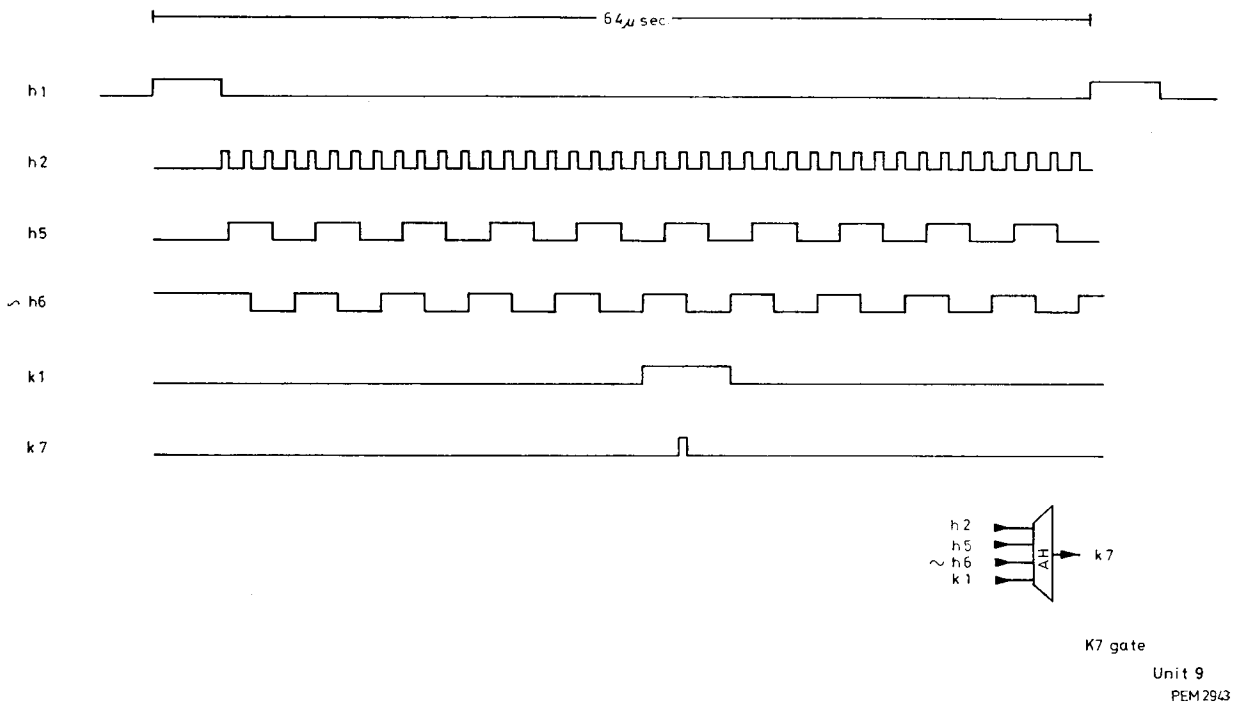


Fig. XV-8 Pulse diagram for "k7"

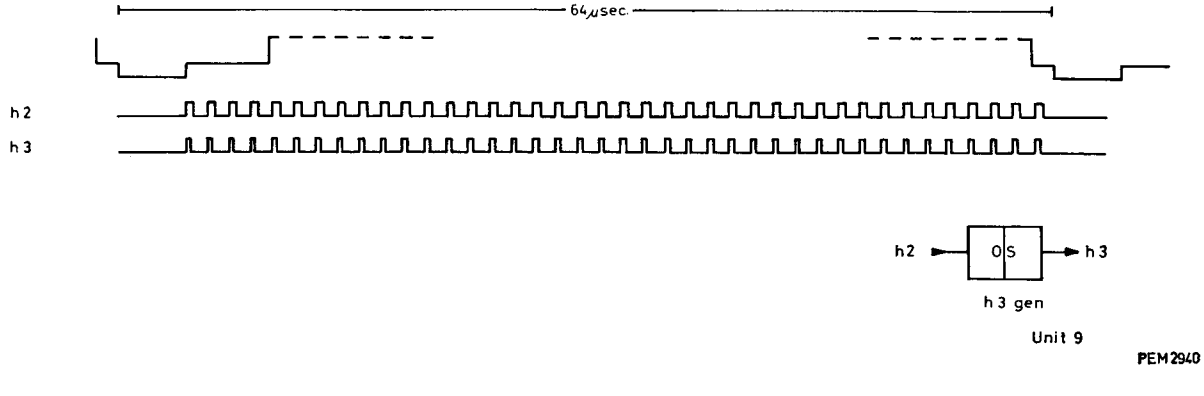


Fig. XV-9 Pulse diagram for "h3"

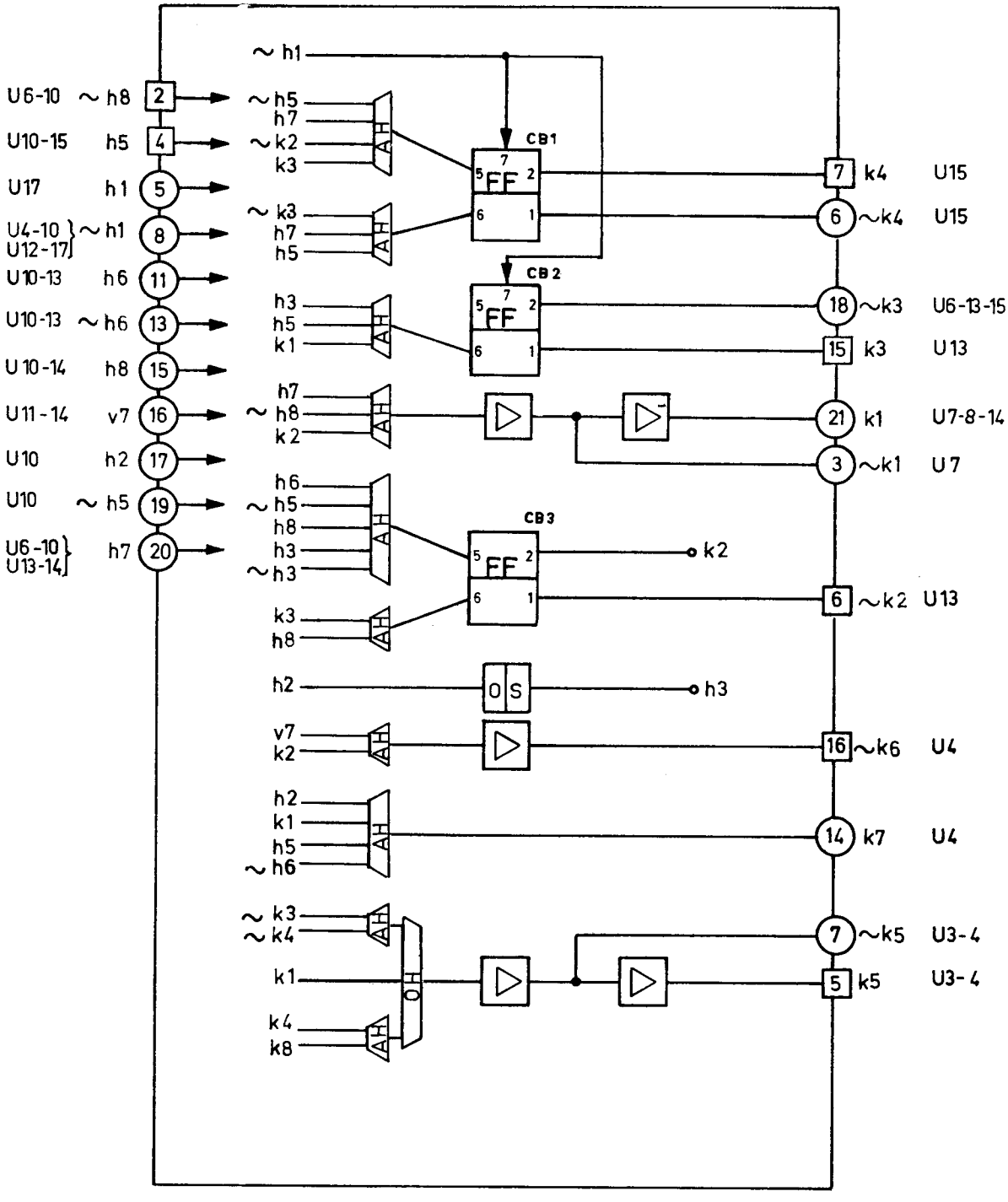


Fig. XV-10 Block-diagram, horizontal decoder, Unit 9

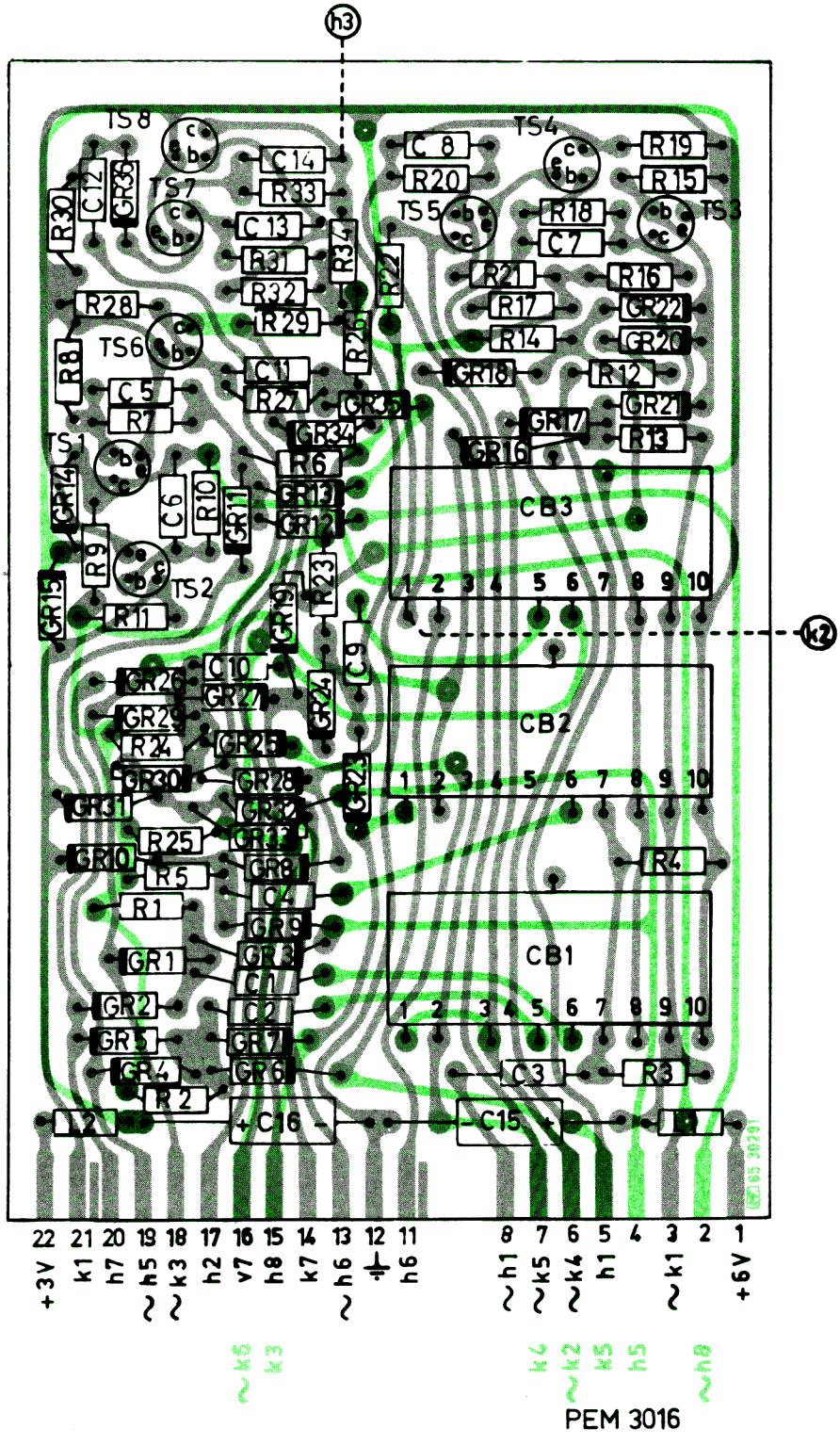
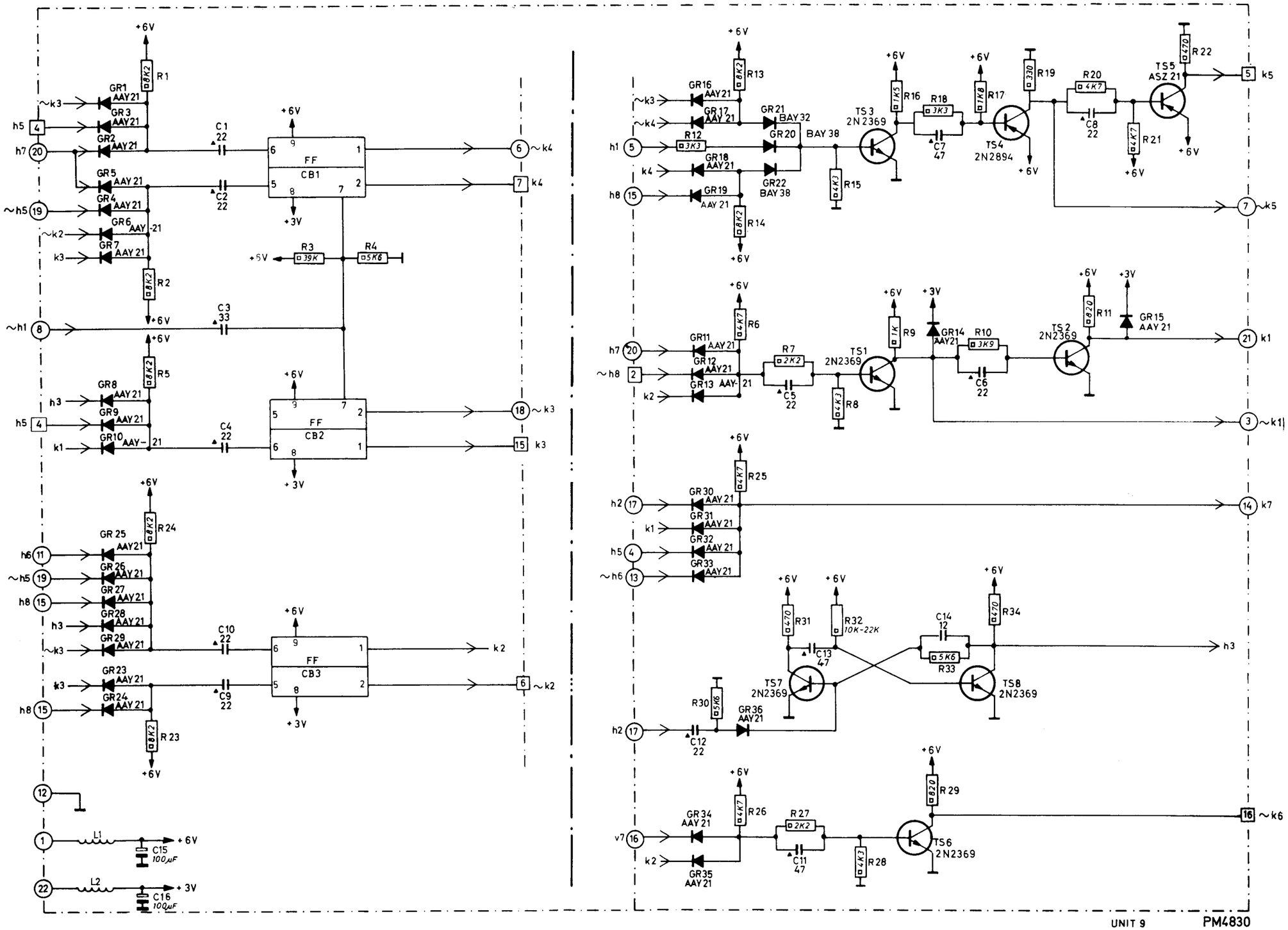


Fig. XV-11 Printed wiring board, horizontal decoder, Unit 9



Erratum: Range R32 should be 6.8kΩ-12kΩ

UNIT 9 PM4830

Fig. XV-12 Circuit diagram, horizontal decoder. Unit 9

XVI Unit 10

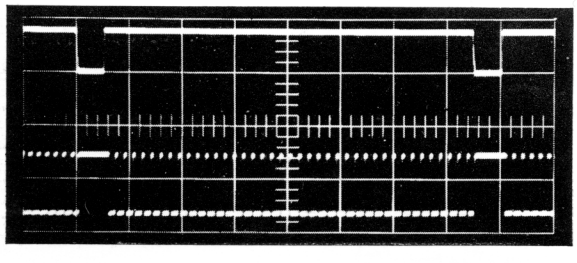
The horizontal divider

This circuit produces pulses to control a number of generators which compose the test patterns.
The circuit consists of a 5 + 1 stage binary divider CB1 . . . CB6 and the 682 kHz[1]) oscillator TS1 and TS2. The feedback of this oscillator is effected via C2, while the frequency is determined by R3 and R4. The oscillator is locked, via TS3, to the line frequency by the line pulse "~ h1".
During the negative "~ h1" pulse TS3 is saturated and TS2 is cut-of, causing the oscillator to stop. During the absence of the "~ h1" pulse TS3 is cut-of and the oscillator is operating.
The peaking circuitry R9-C4 is used for obtaining a correct pulse shape.
The oscillated pulses are applied to TS4 and TS5 and to the dividers CB1 . . . CB6. These dividers are set to zero for each line by means of the "~ h1" pulse via reset input 7, so that the generated pulses will have the same phase in all lines. The generated pulses "h2", "h5", "~ h5", "h6", "~ h6", "h7", "h8" and "~ h8" arre applied to the horizontal decoder (unit 9), the "h7", "~ h8" and "~ h9" pulses to the line decoder (unit 6). The "h5" and "~ h4" pulses are also applied to the cross-bar gate (unit 15), the "h7", "h8" and "h9" pulses to the linear gate (unit 14) and the "h6", "~ h6" and "h7" pulses to the black/white step generator (unit 13).

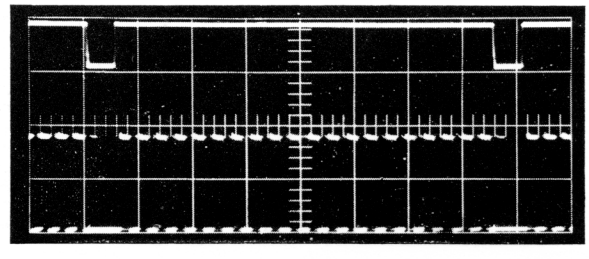
Checking and adjusting
Measuring equipment:
Oscilloscope: e.g. PHILIPS PM 3330.

Frequency of horizontal oscillator (682 kHz)
Connect oscilloscope to "OUTPUT II".
The width of the black/white steps ("h5" pulse) at the left and right-hand side of the pattern should be 4.0 µs for PM5540/E and 4.5 µs for PM5540/A.
If not, select R4 (2.2 kΩ – 3.9 kΩ).

[1]) For PM5540/A read: 687 kHz

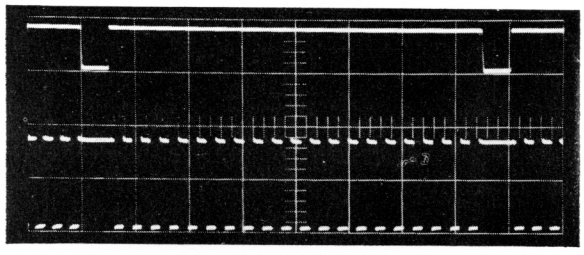


h2
5 V/cm 8 µs/cm
reference: line sync.

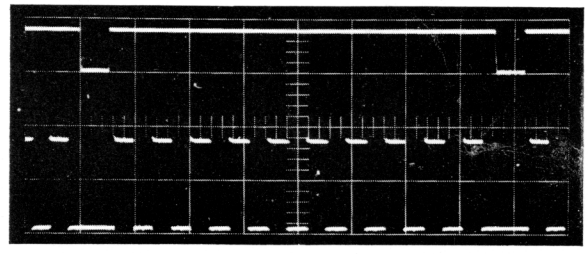


h4
2 V/cm 8 µs/cm
reference: line sync.

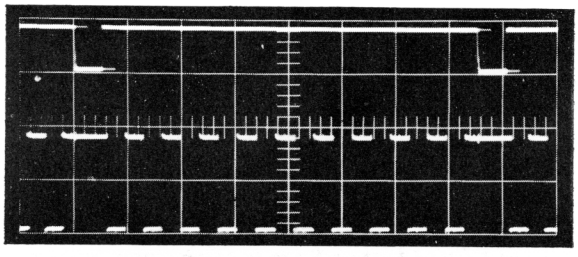
Fig. XVI-1 Oscillograms, Unit 10



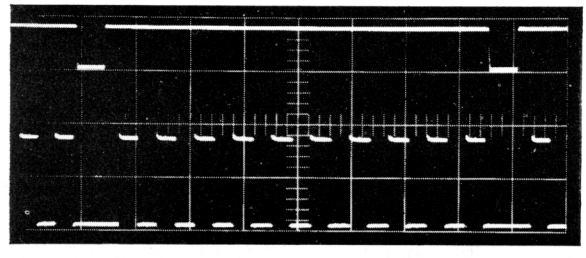
~ h4
2 V/cm 8 µs/cm
reference: line sync.



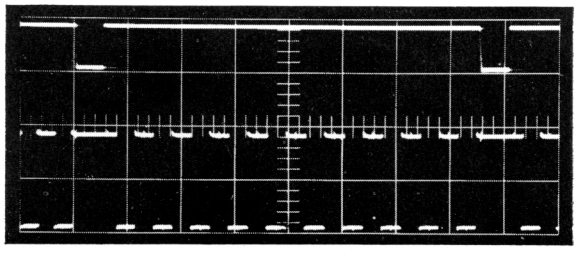
h5
2 V/cm 8 µs/cm
reference: line sync.



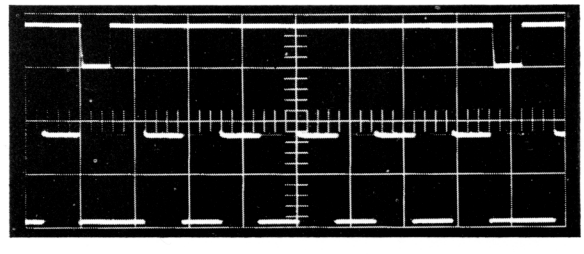
~ h5
2 V/cm 8 µs/cm
reference: line sync.



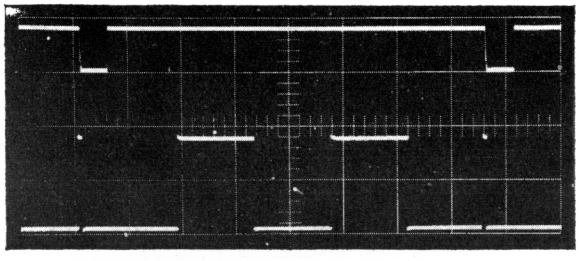
h6
2 V/cm 8 µs/cm
reference: line sync.



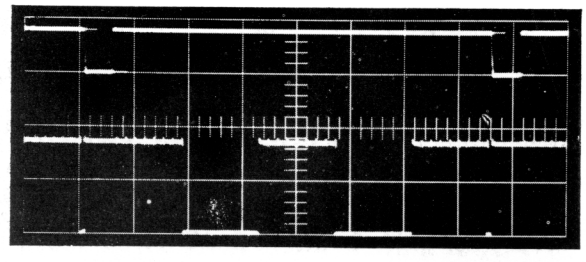
~ h6
2 V/cm 8 µs/cm
reference: line sync.



h7
2 V/cm 8 µs/cm
reference: line sync.

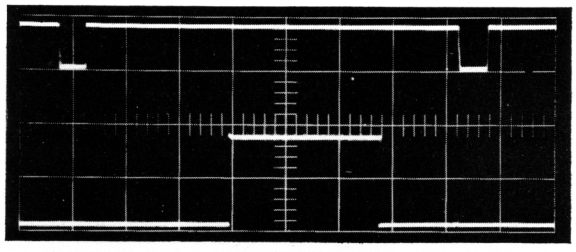


h8
2 V/cm 8 µs/cm
reference: line sync.

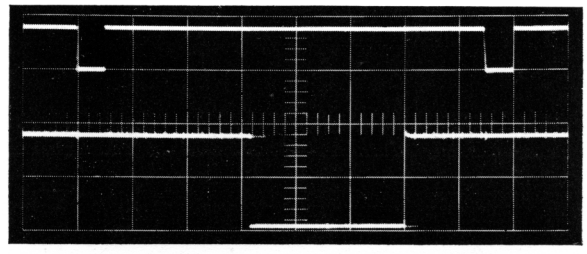


~ h8
2 V/cm 8 µs/cm
reference: line sync.

Fig. XVI-1 Oscillograms, Unit 10

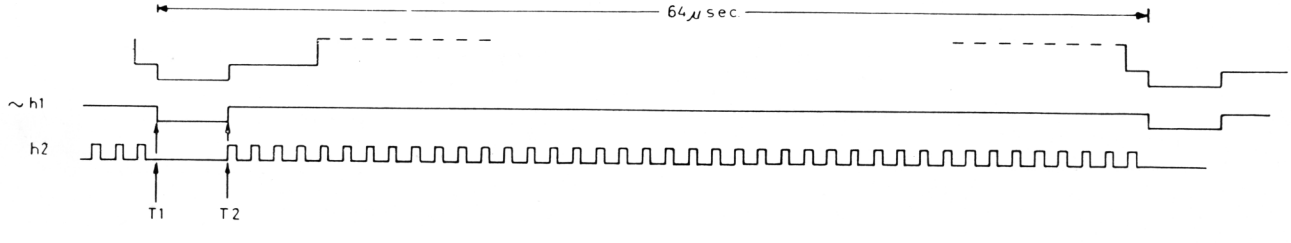


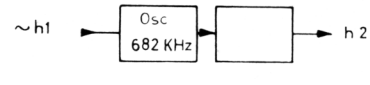
h9
2 V/cm 8 µs/cm
reference: line sync.



~ h9
2 V/cm 8 µs/cm
reference: line sync.

Fig. XVI-1 Oscillograms, Unit 10





h2 gen.

Unit 10
PEM 4820

Fig. XVI-2 Pulse diagram for "h2"

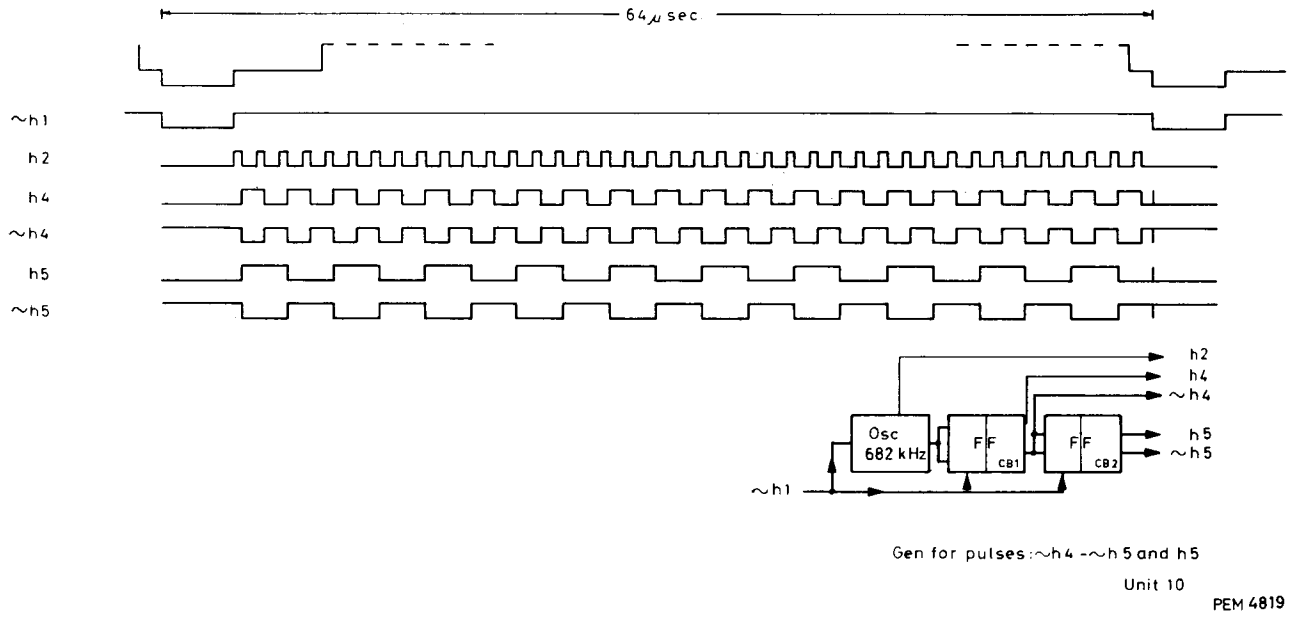


Fig. XVI-3 Pulse diagrams for "~ h4", "h5" and "~ 5"

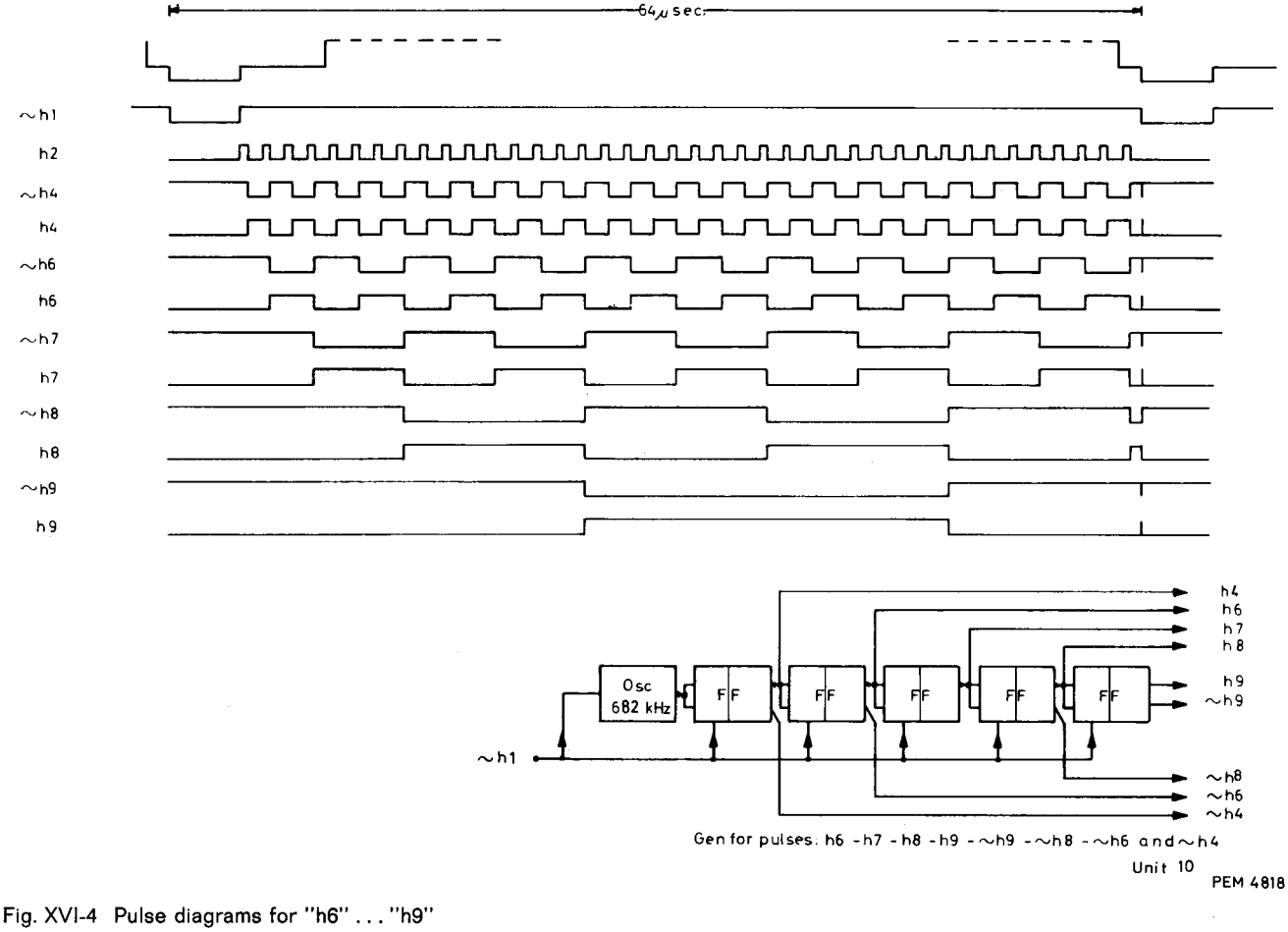


Fig. XVI-4 Pulse diagrams for "h6" . . . "h9"

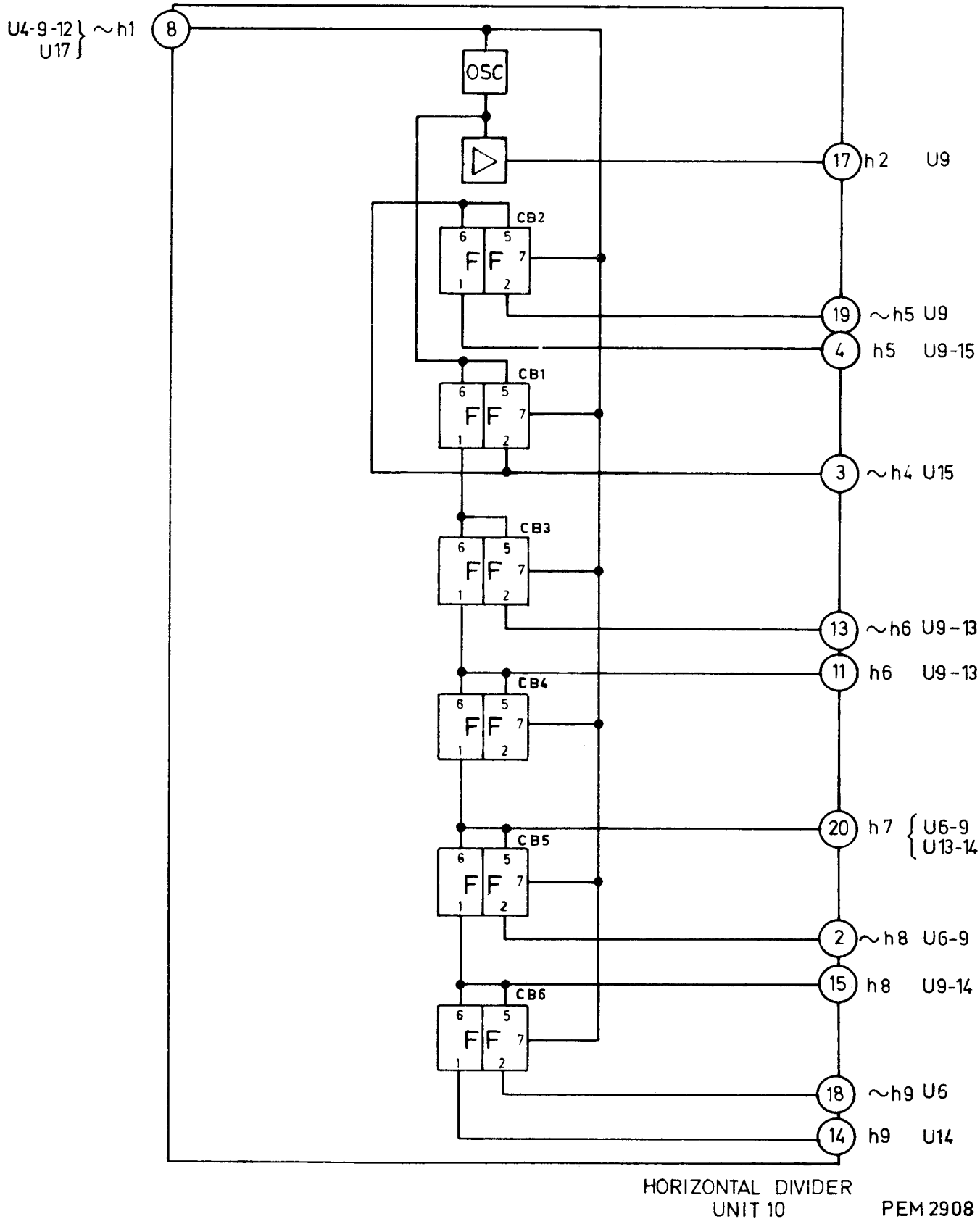


Fig. XVI-5 Block-diagram, horizontal divider, Unit 10

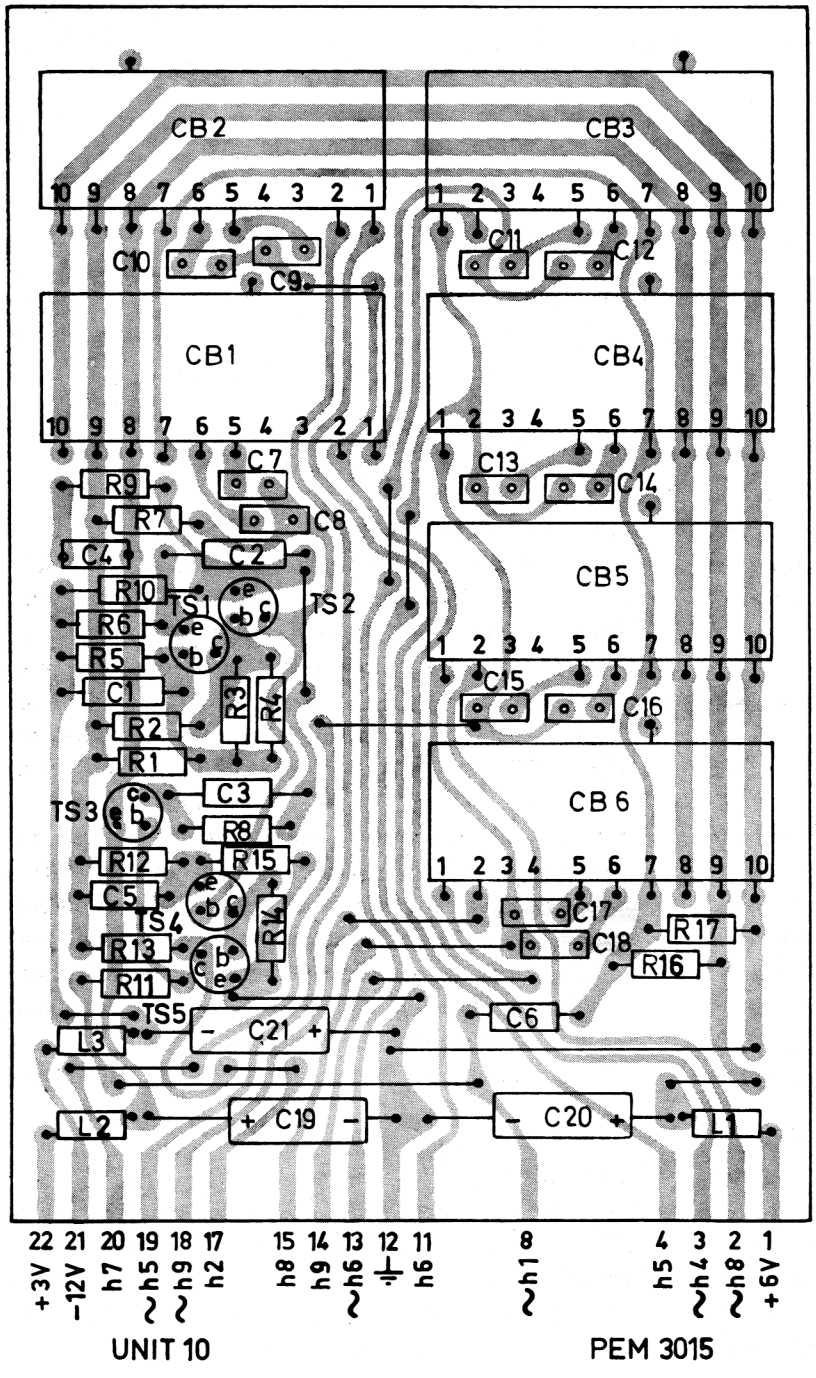


Fig. XVI-6 Printed wiring board, horizontal divider, Unit 10

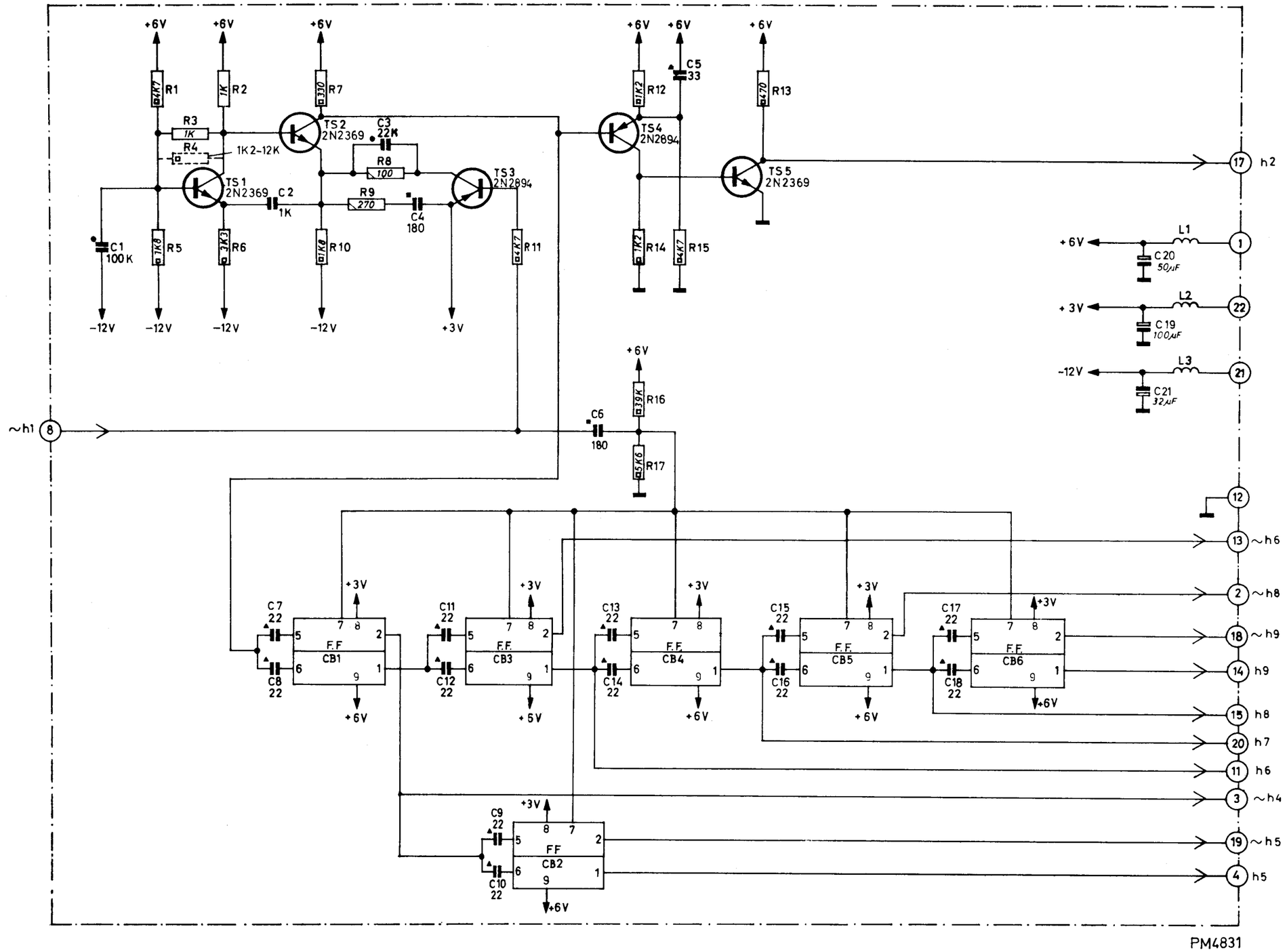


Fig. XVI-7 Circuit diagram, horizontal divider, Unit 10

XVII Unit 11

The vertical decoder

The purpose of the decoder is to supply the vertical gating pulses. These pulses, based on pulses from the vertical divider (unit 12), are produced by a group of generators.

Generator for the "v2", "v3", "v4", "v5" and "v6" pulses

The pulses are produced in the flip-flops CB2 . . . CB6 which function as a shift register.

First all flip-flops are set to zero by the "∿ f1" pulse.

Then the "∿ f8" pulse is applied to input 5, but as these flip-flops are set to zero, they are not influenced by the "∿f8" pulse. Due to the action of the combined pulses "∿ v1", "∿ f8" and "∿ v7" in the AND-gates GR7 . . . GR9, flip flop CB2 changes from state "0" to state "1".

When the first negative step of the "∿ f8" pulse appears, CB2 changes into the other stable state. At the next negative step of the "∿ f8" pulse CB8 changes, etc. so that the information of each flip-flop shifts one place upwards, untill they all in turn are activated.

The generated pulses "v2" . . . "v6" are applied to the interval decoder (unit 8), the "v2", "v4" and "v6" pulses to the black/white step generator (unit 13) and "v3", "v4", "v5" and "v6" pulses to the linear-gate (unit 14). The "v4" pulse is also applied to the "g4" and "∿ g4" generator in unit 17.

Generator for the "v1" pulse

This generator consists of the flip-flop CB1, the AND-gate GR1 . . . GR4 and GR5 . . . GR6 combined with GR11 . . . GR14 (unit 12) producing the "v9" pulse.

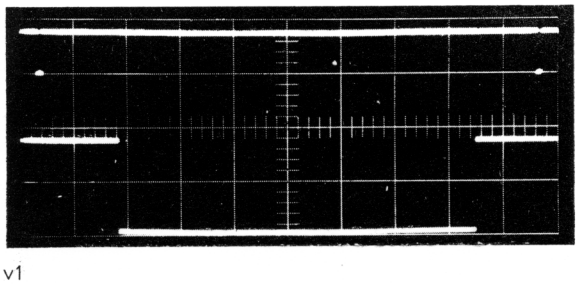
The "reset" of CB1 (input 6) is controlled by the gate output pulses of GR1 . . . GR4 ("f6", "f7", "∿ f8" and "∿ g4"), and "set" (input 5) by the output pulses of GR5 . . . GR6 and GR11 . . . GR14 "f8", "∿ v7" and "v9" ("v9" = "∿ f3", "∿ f4", "∿ f5" and "∿ f7").

In circumstances that the generator is not reset at the beginning of a field (e.g. after switching) the "∿ f1" pulse ensures that this will be done. The gate output pulse on input 5 cannot trigger the flip-flop. When the first negative step appears at input 6, flip-flop changes its state until the next negative step at input 5 causes the flip-flop to change its state again.

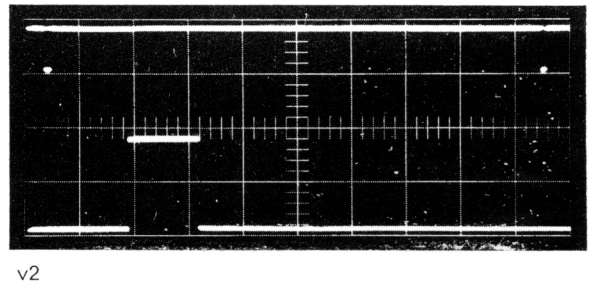
The "v1" and "∿ v1" pulses are applied to the Cross-bar gate (unit 15).

Generator for the "v7" pulse

The "v7" and "∿ v7" pulses are produced by flip-flop CB7 of which the "set" and "reset" inputs are controlled by the "∿ v2" and "v6" pulses. In circumstances that the generator is not reset at the beginning of a field (e.g. after-switching), the "∿ f1" pulse ensures that this will be done. The "v7" pulse is applied to units 9 and 14 and the "∿ v7" pulse to units 8 and 13.

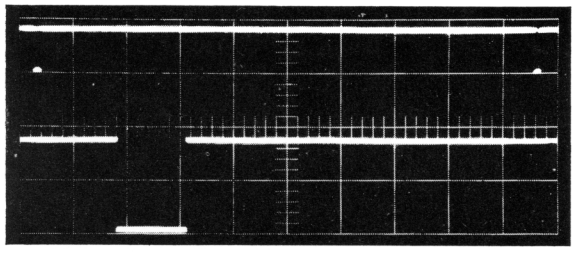


v1
2 V/cm 2 ms/cm
reference: frame sync.

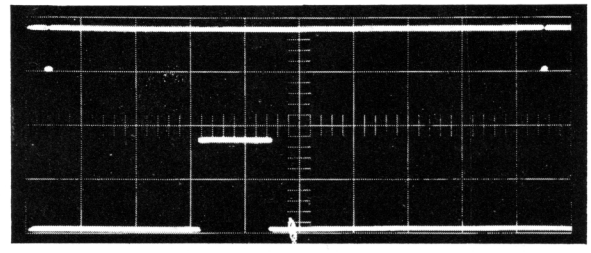


v2
2 V/cm 2 ms/cm
reference: frame sync.

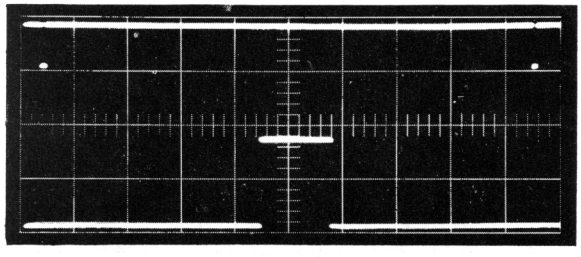
Fig. XVII-1 Oscillograms, Unit 11



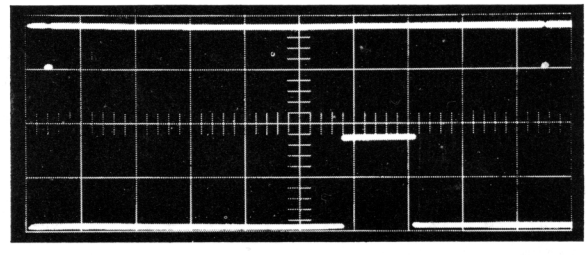
~ v2
2 V/cm 2 ms/cm
reference: frame sync.



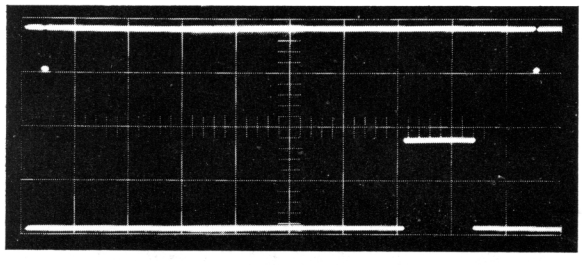
v3
2 V/cm 2 ms/cm
reference: frame sync.



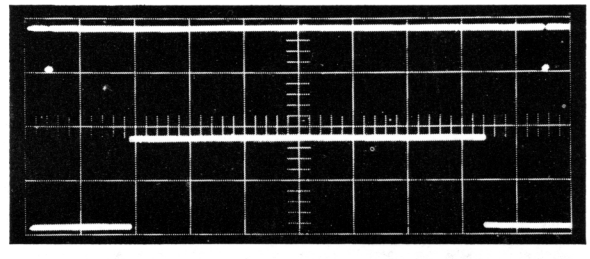
v4
2 V/cm 2 ms/cm
reference: frame sync.



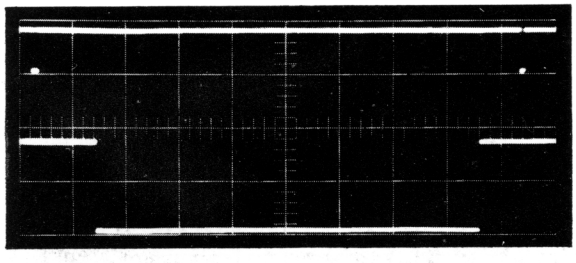
v5
2 V/cm 2 ms/cm
reference: frame sync.



v6
2 V/cm 2 ms/cm
reference: frame sync.



v7
2 V/cm 2 ms/cm
reference: frame sync.



~ v7
2 V/cm 2 ms/cm
reference: frame sync.

Fig. XVII-1 Oscillograms, Unit 11

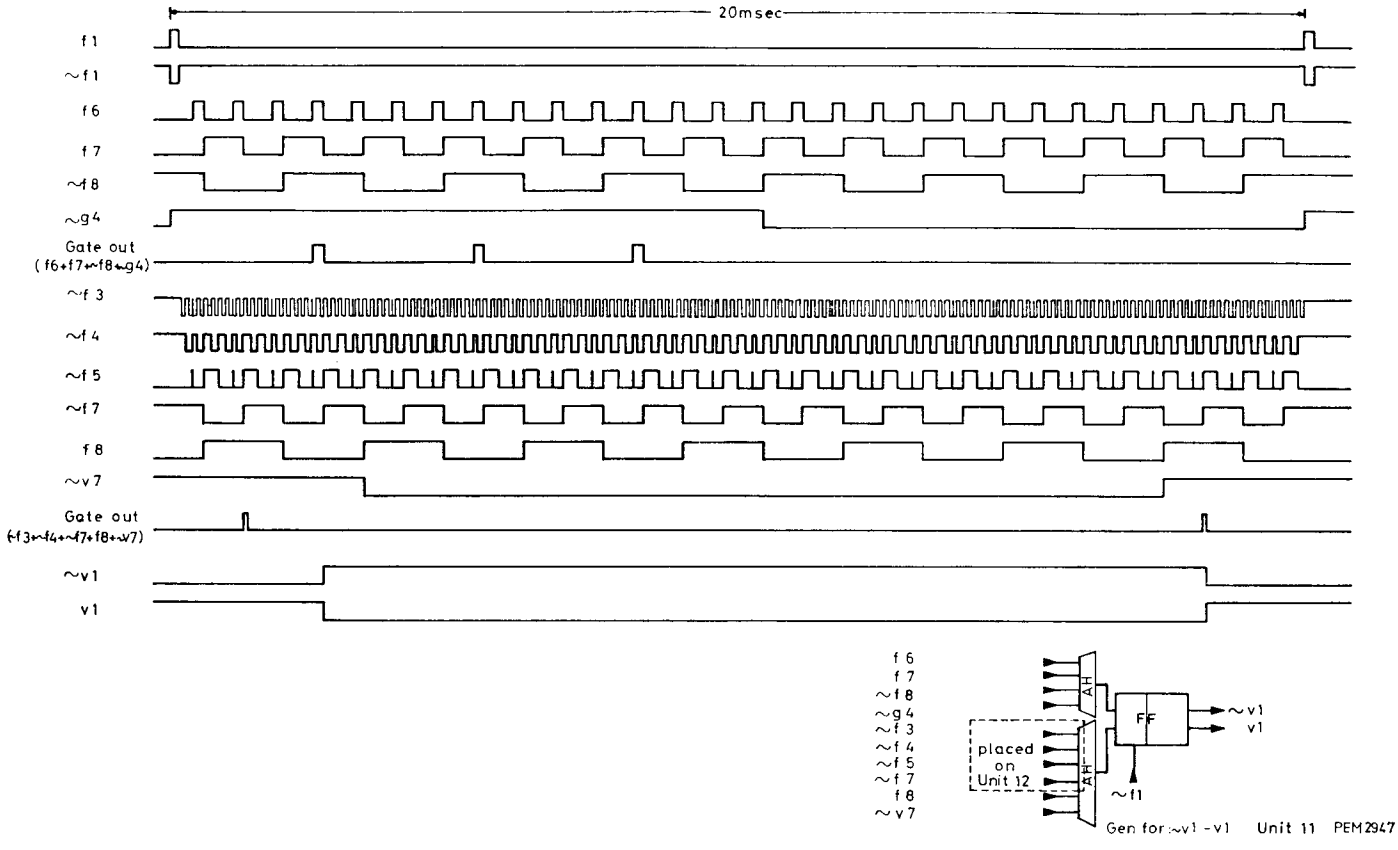


Fig. XVII-2 Pulse diagrams for "v1" and "~ v1"

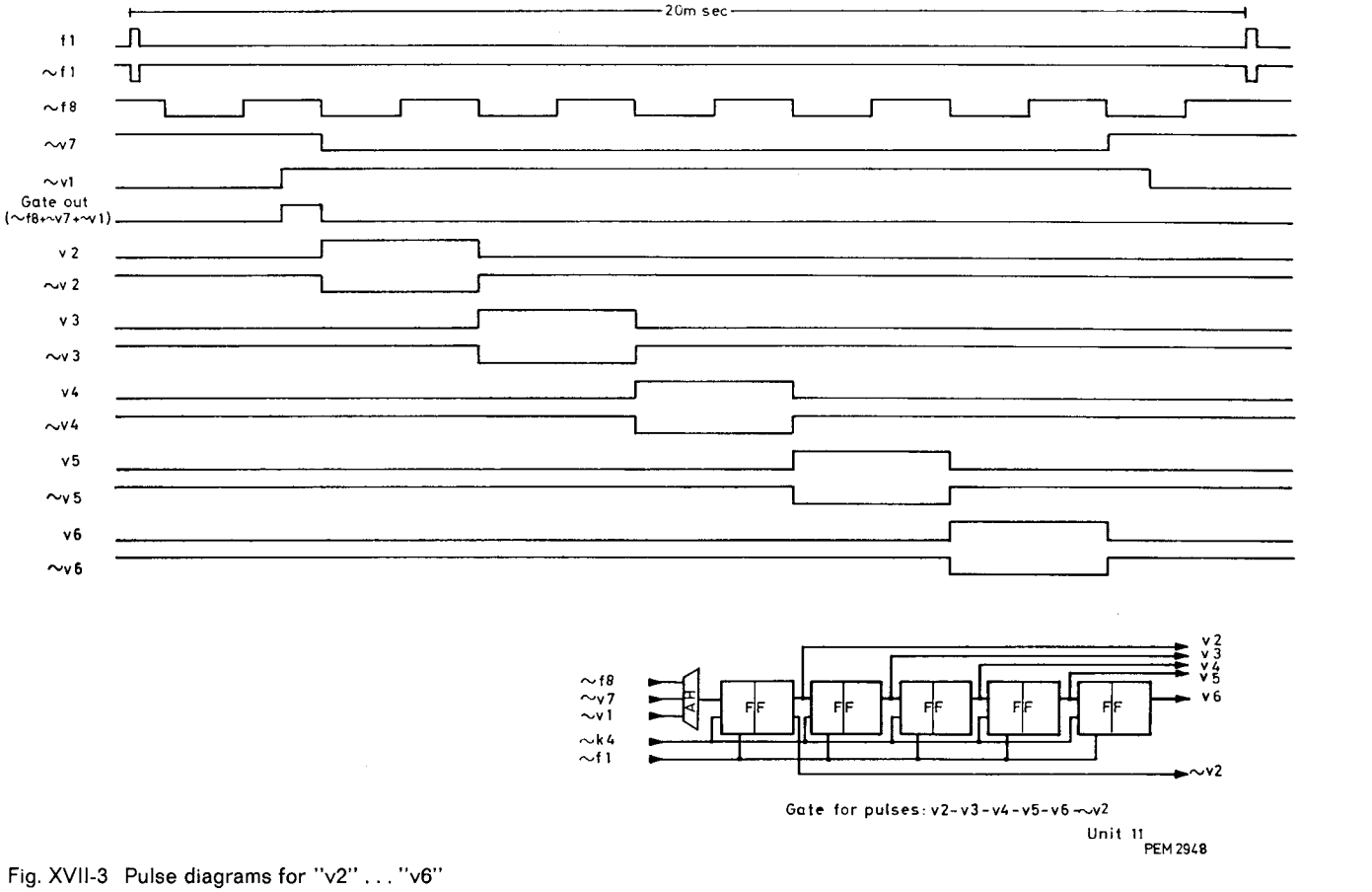


Fig. XVII-3 Pulse diagrams for "v2" . . . "v6"

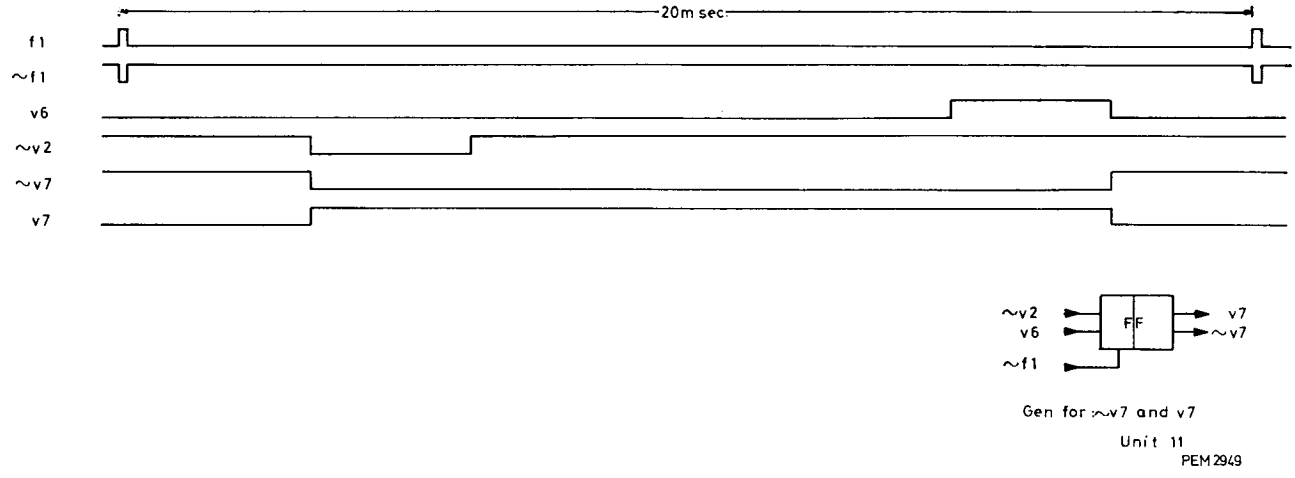


Fig. XVII-4 Pulse diagrams for "v7" and "~ v7"

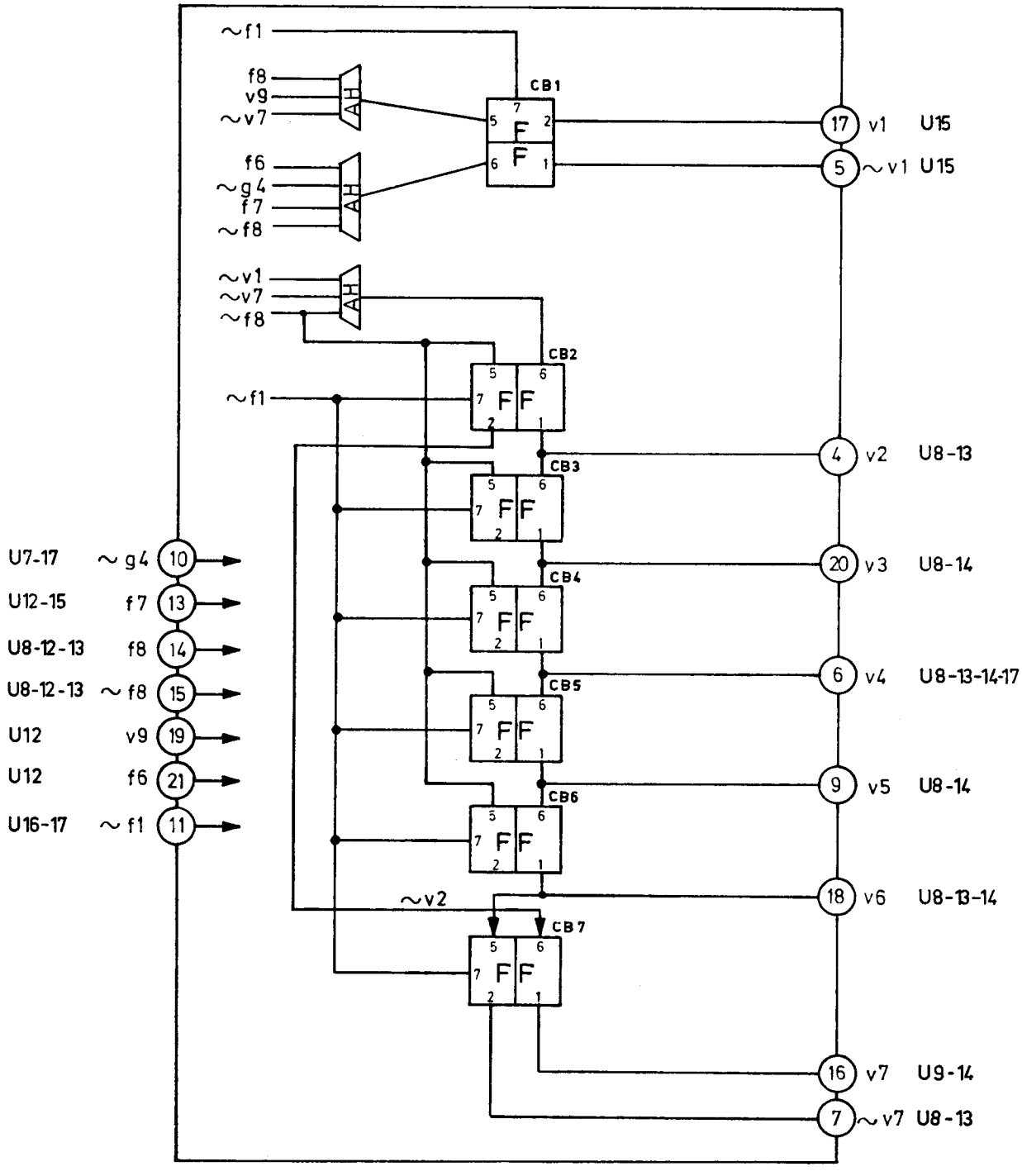


Fig. XVII-5 Block-diagram, vertical decoder, Unit 11

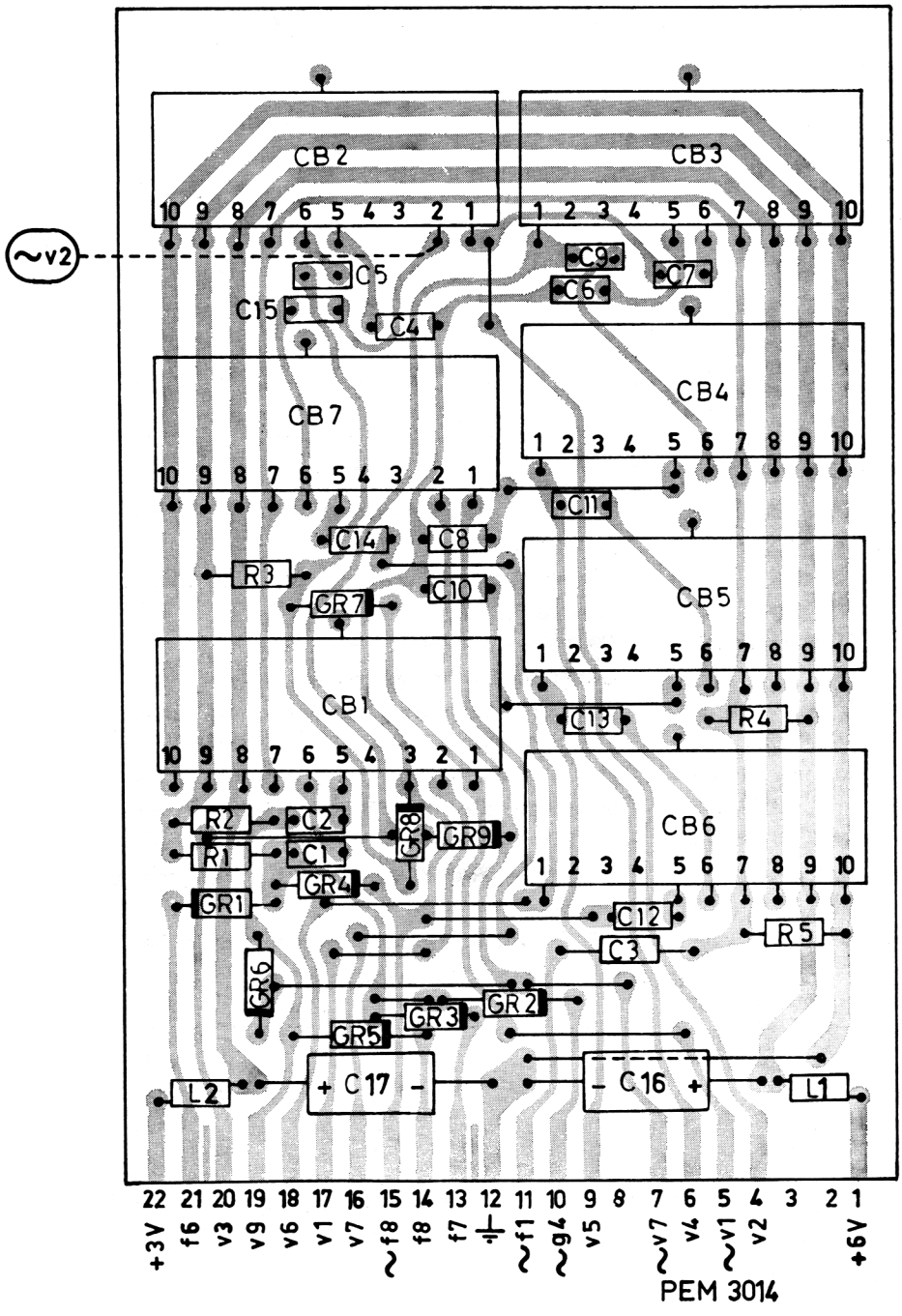


Fig. XVII-6 Printed wiring board, vertical decoder, Unit 11

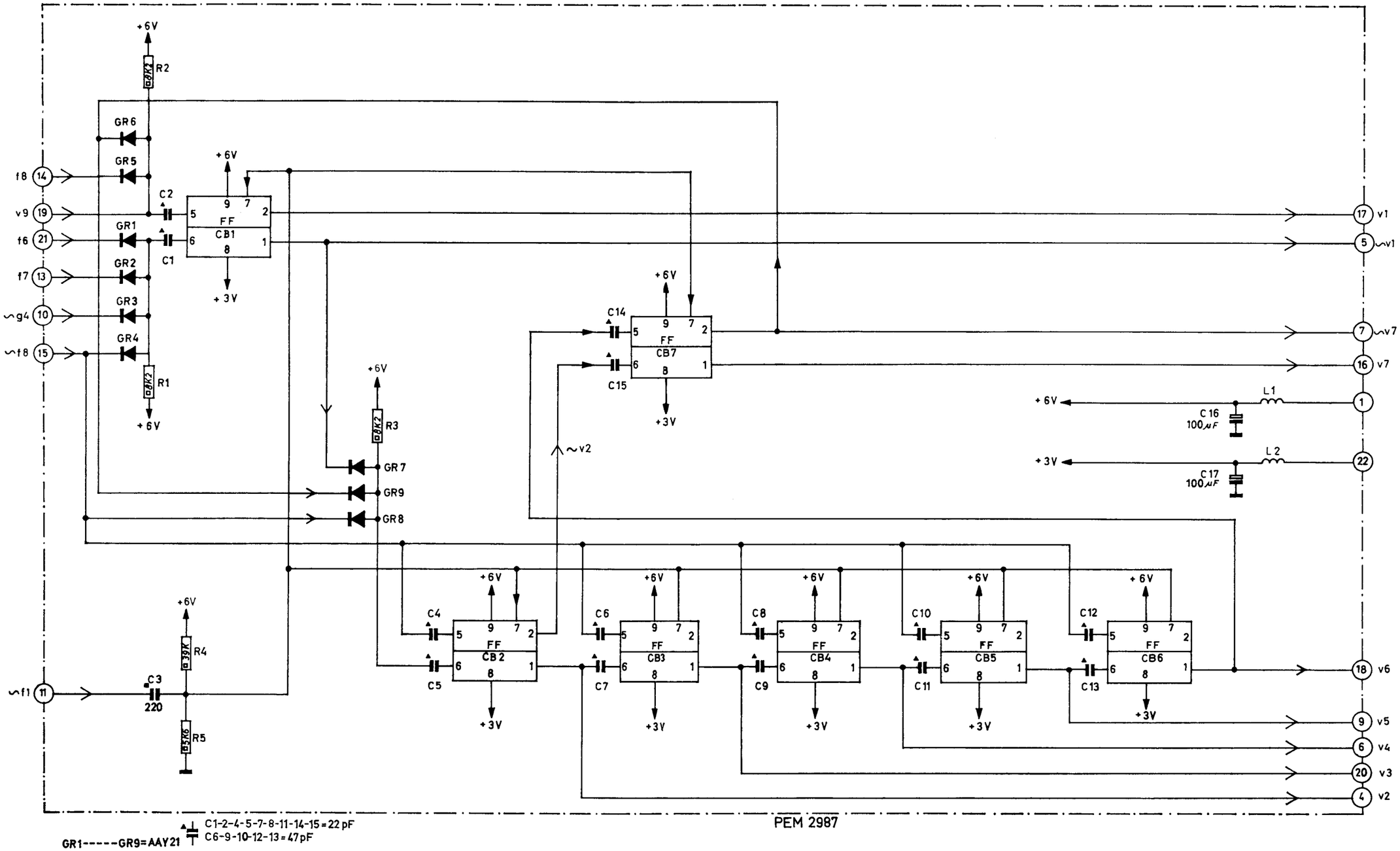


Fig. XVII-7 Circuit diagram, vertical decoder, Unit 11

XVIII Unit 12

The vertical divider

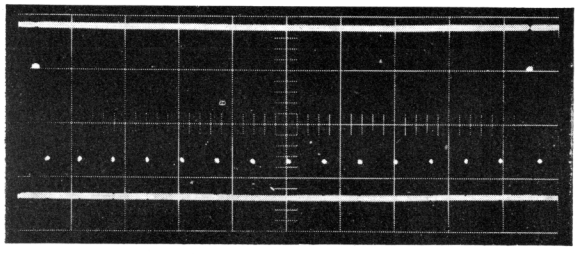
This circuit produces pulses which, after decoding drive a number of generators used to generate the gating pulses for the test patterns.

The circuit is built up as a 6 stage divider which counts pulses of the line frequency ("∿ h1").
The flip-flops CB1 . . . CB4 form a 11:1[1]) divider by feeding back the "∿ f6" pulse to CB1 and CB3. Flip-flop CB5 produces the "f7" pulse which is repeated every 22 lines. Flip-flop CB6 produces the "f8" pulse which, in combination with the gate pulses of units 8 and 13, is used for dividing the circle into 10 intervals. To get the pulses in the correct mutual phase, the divider is set each frame by the "f2" pulse, after the "∿ h1" pulse, present at the same time, has disappeared.
CB1, 2, 4, 5 and 6 are set to state "0" while CB3 is set to state "1".

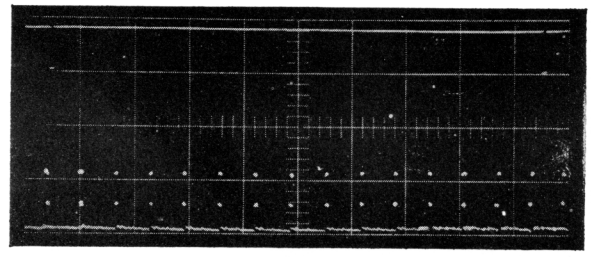
Generator for the "g2" pulse
This generator, which supplies the "g2" pulse, consists of the AND-gate GR7-GR10 and the amplifier TS1 . . . TS2. This pulse, which is clamped to +3 V by GR19, is applied to the units 7, 8 and 17.

The AND-gate GR11 . . . GR14, supplying the "v9" pulse is used in unit 11.
The AND-gate GR15 . . . GR18, supplying the "v8" pulse is used in unit 15.

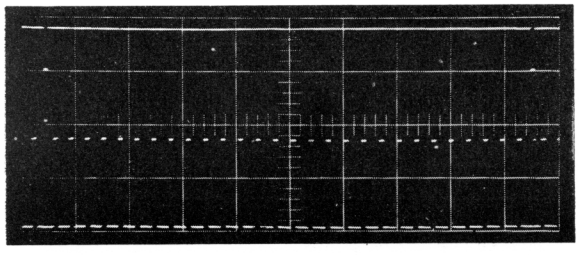
[1]) For PM5540/A read 9:1



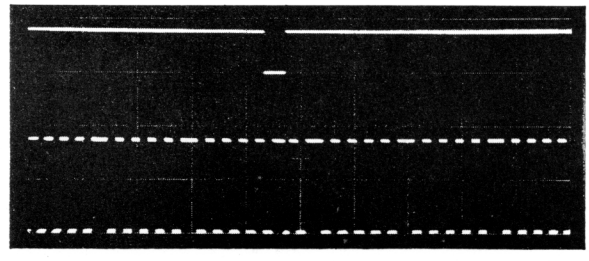
g2
5 V/cm 2 ms/cm
reference: frame sync.



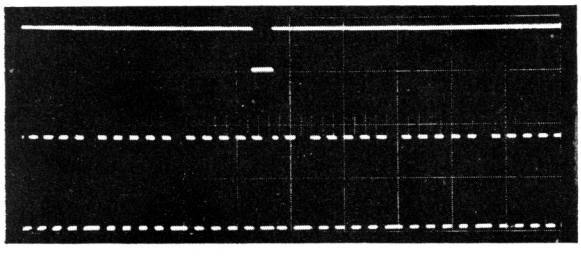
v8
2 V/cm 2 ms/cm
reference: frame sync.



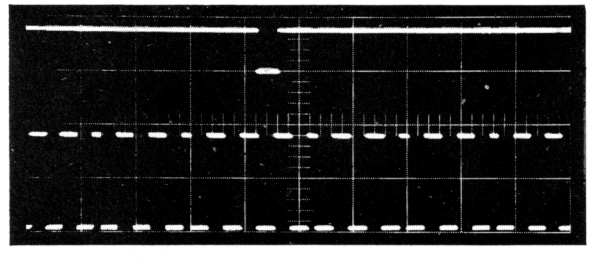
v9
2 V/cm 2 ms/cm
reference: frame sync.



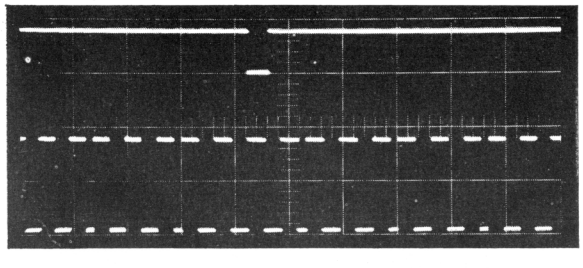
f3
2 V/cm 400 µs/cm
reference: frame sync.



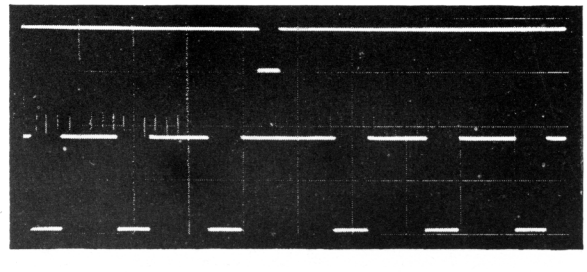
~ f3
2 V/cm 400 µs/cm
reference: frame sync.



~ f4
2 V/cm 400 µs/cm
reference: frame sync.

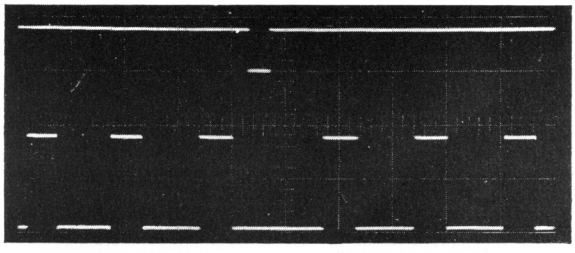


f4
2 V/cm 400 µs/cm
reference: frame sync.

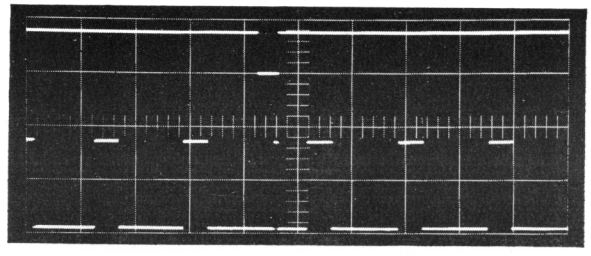


f5
2 V/cm 400 µs/cm
reference: frame sync.

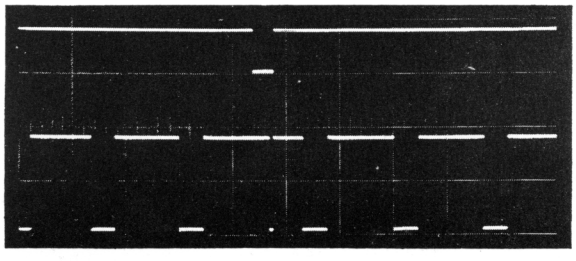
Fig. XVIII-1 Oscillograms, Unit 12



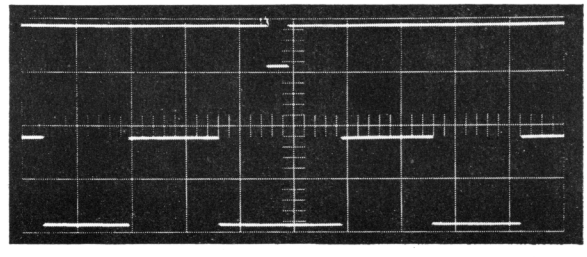
~ f5
2 V/cm 400 µs/cm
reference: frame sync.



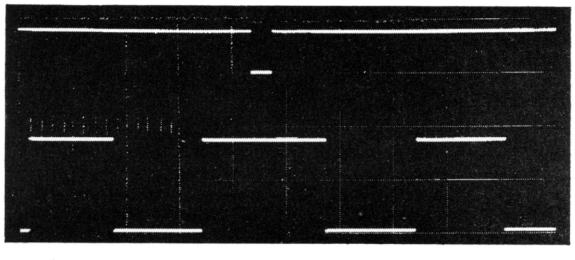
f6
2 V/cm 400 µs/cm
reference: frame sync.



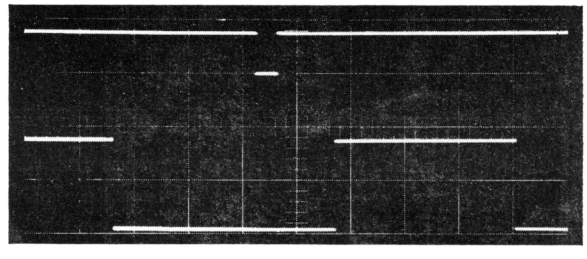
~ f6
2 V/cm 400 µs/cm
reference: frame sync.



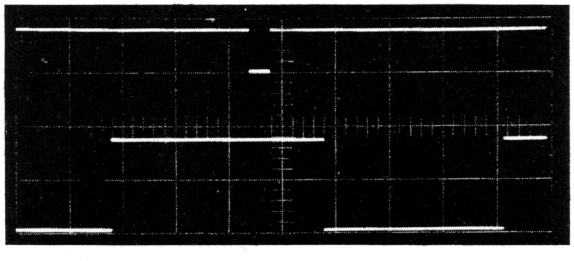
f7
2 V/cm 400 µs/cm
reference: frame sync.



~ f7
2 V/cm 400 µs/cm
reference: frame sync.



f8
2 V/cm 400 µs/cm
reference: frame sync.



~ f8
2 V/cm 400 µs/cm
reference: frame sync.

Fig. XVIII-1 Oscillograms, Unit 12

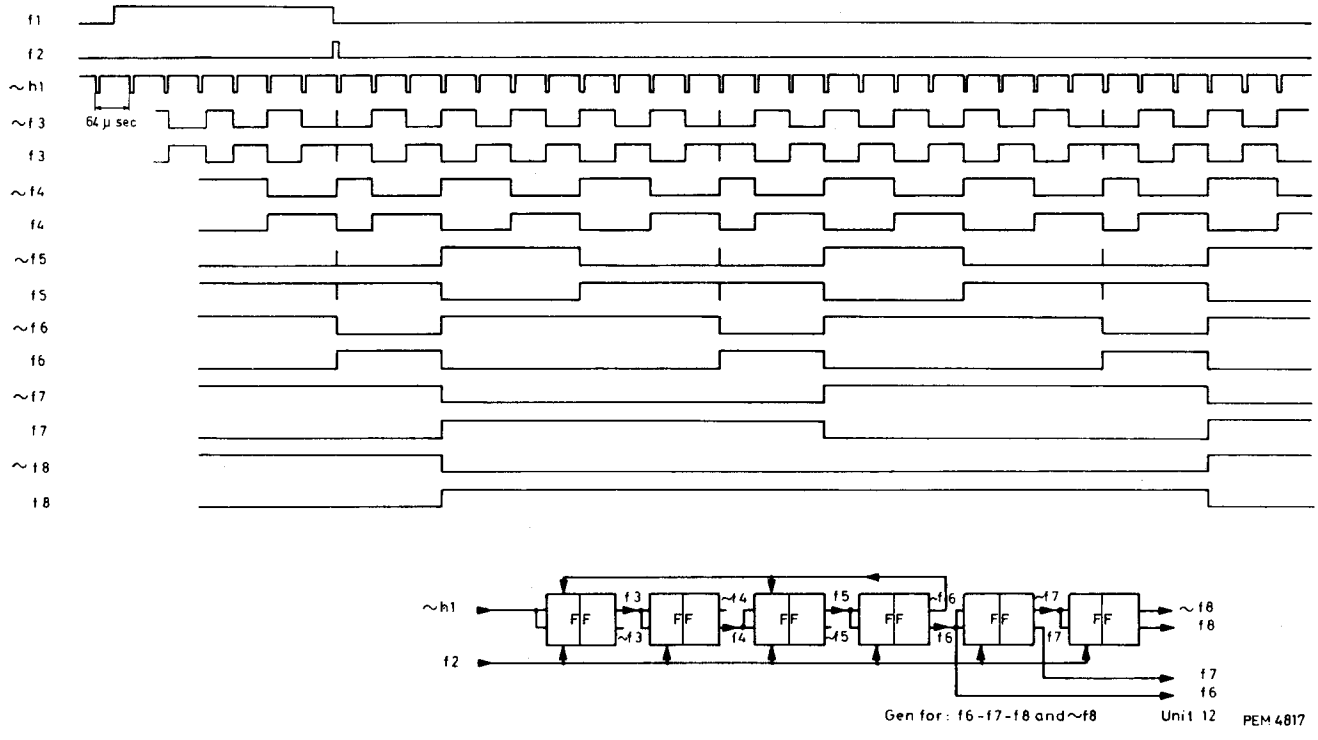


Fig. XVIII-2 Pulse diagrams for "f6", "f7", "f8" and "$\sim$ f8"

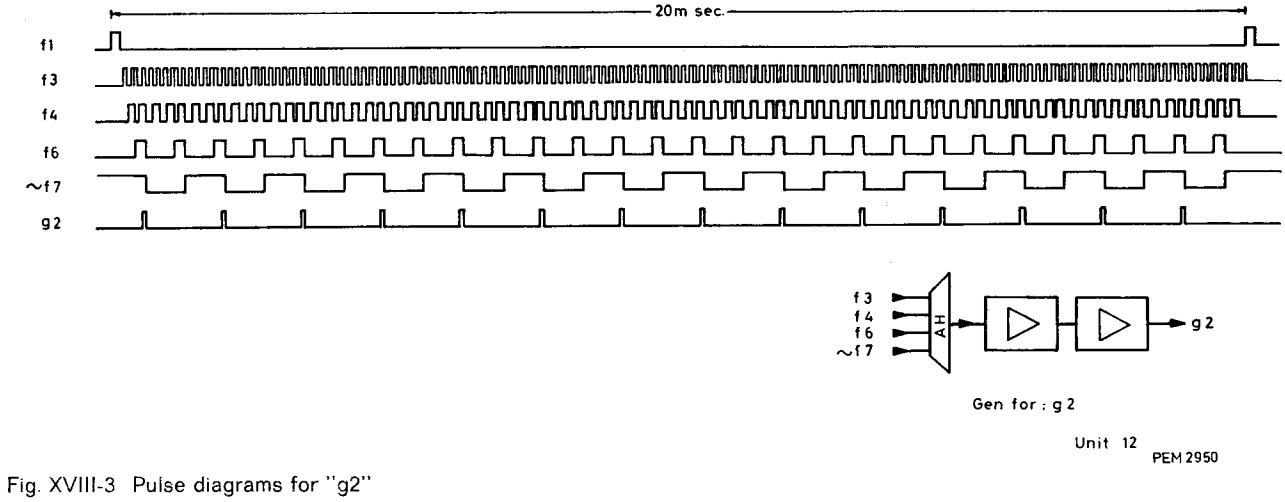


Fig. XVIII-3 Pulse diagrams for "g2"

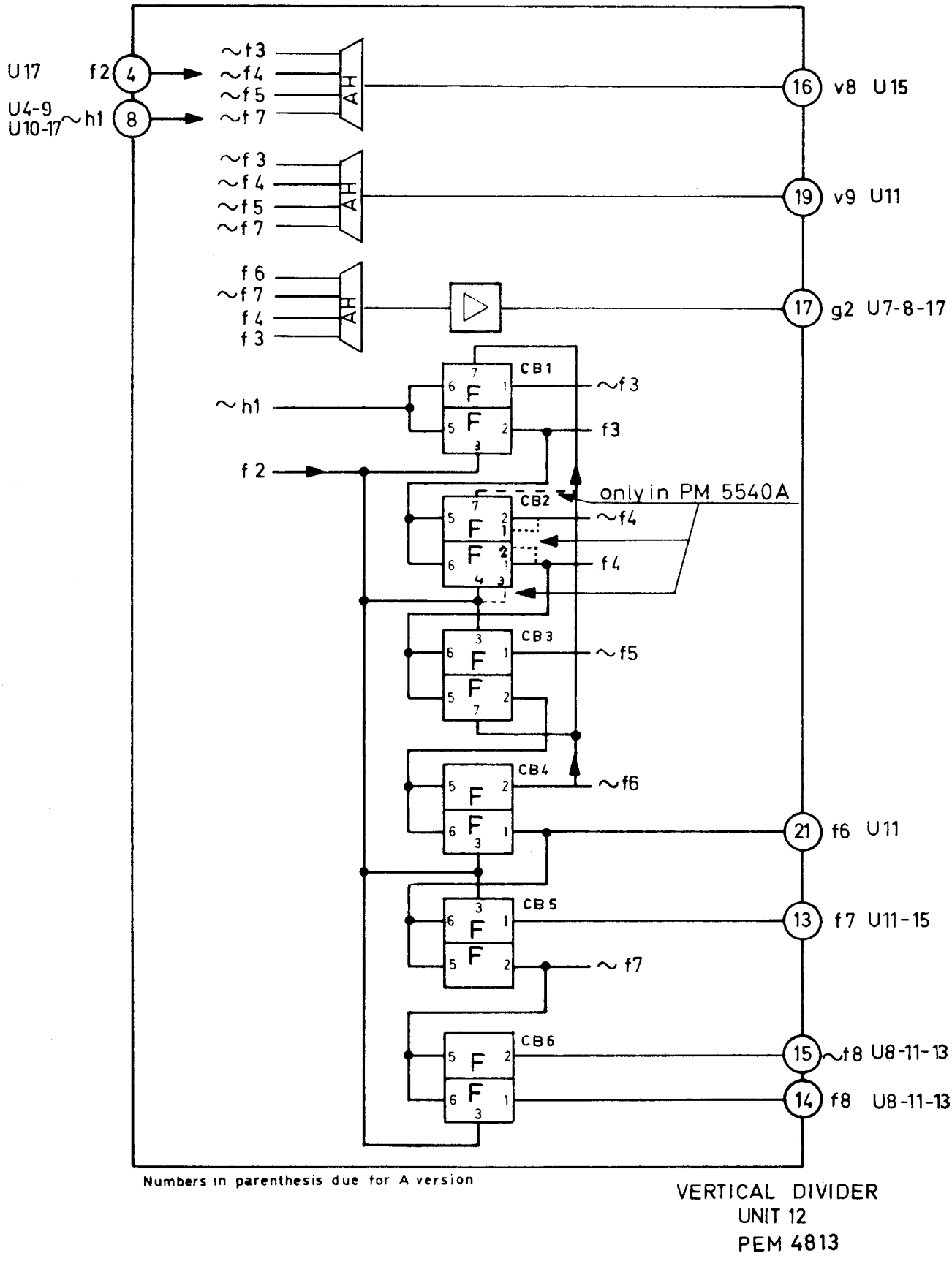


Fig. XVIII-4 Block-diagram, vertical divider, Unit 12

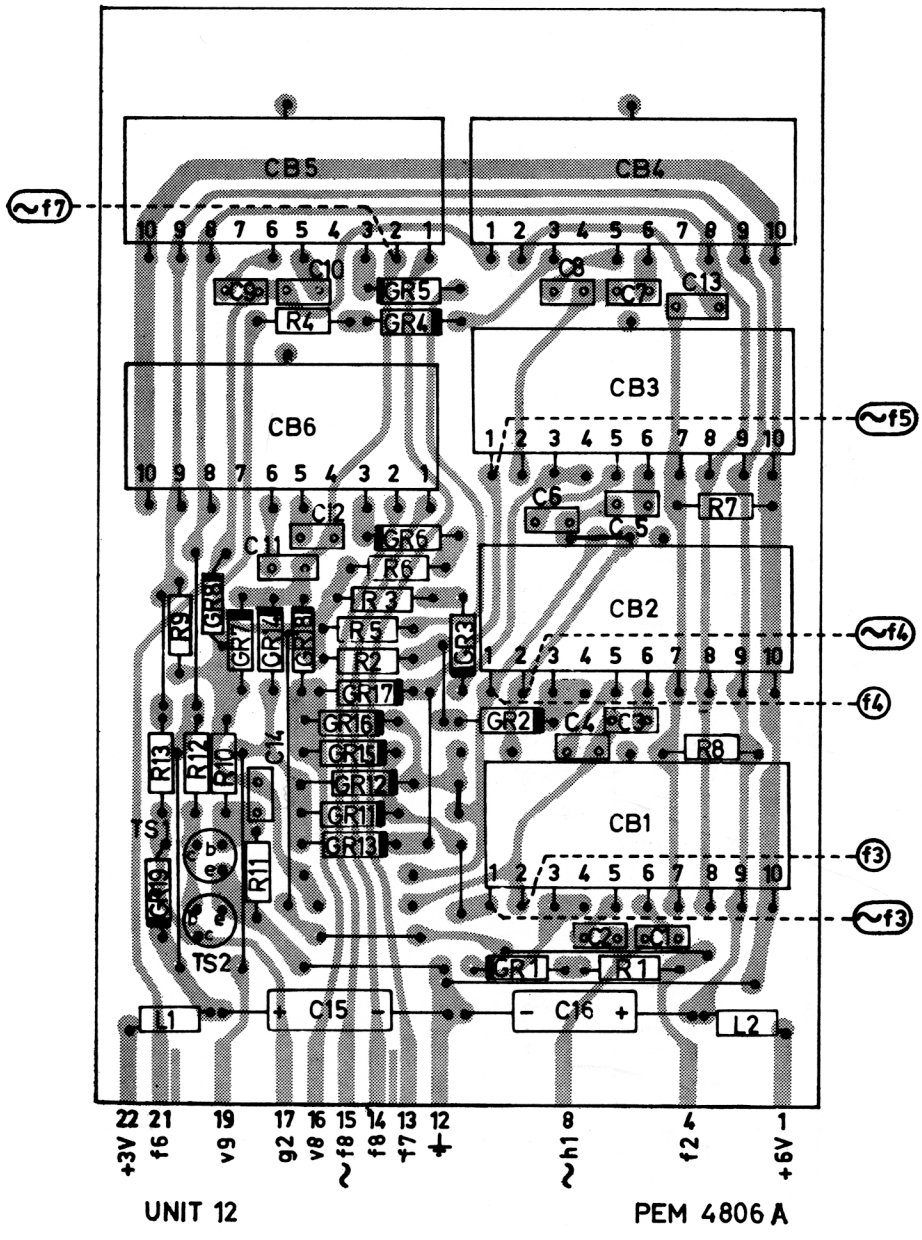


Fig. XVIII-5a Printed wiring board, vertical divider (A version), Unit 12

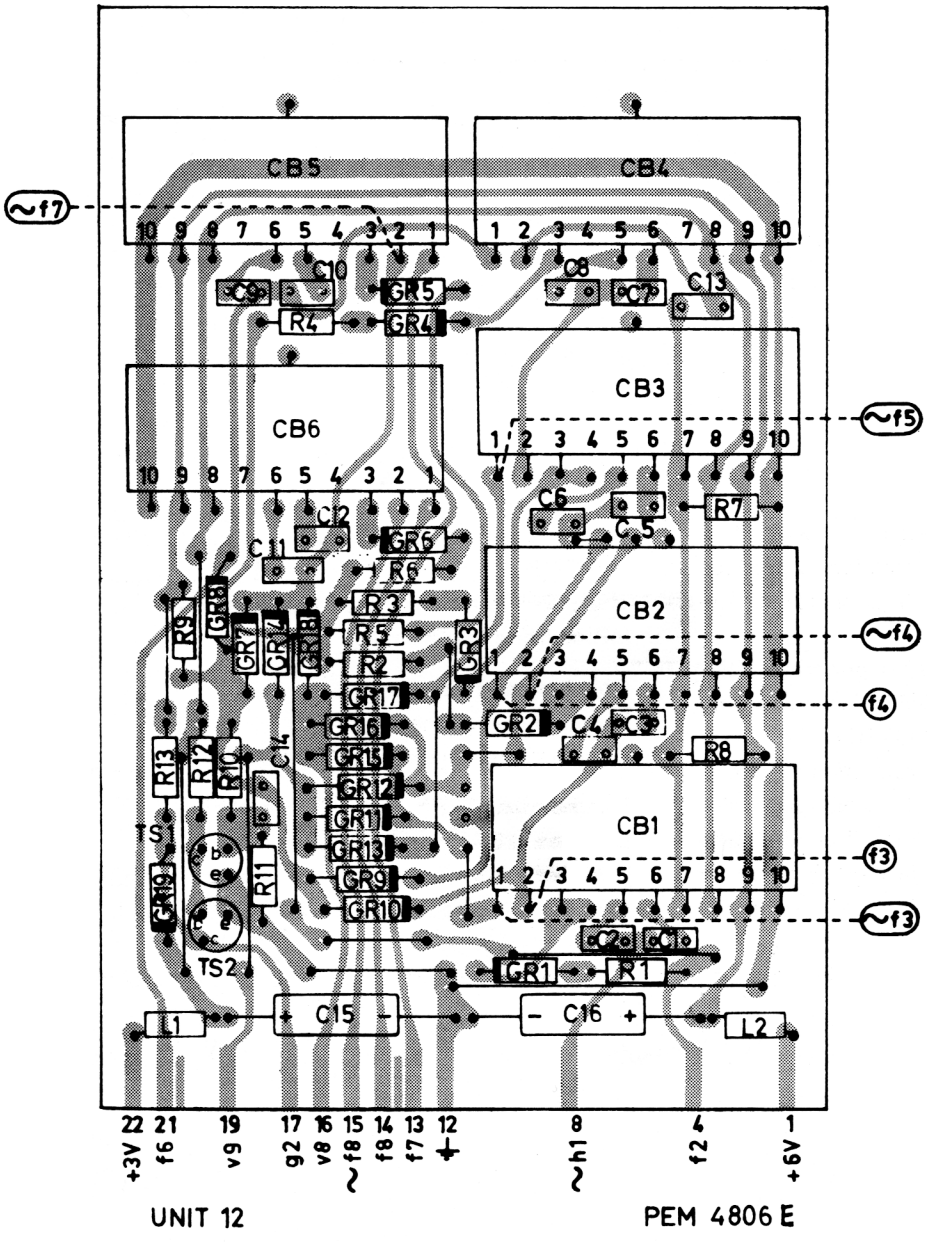


Fig. XVIII-5b Printed wiring board, vertical divider (E version), Unit 12

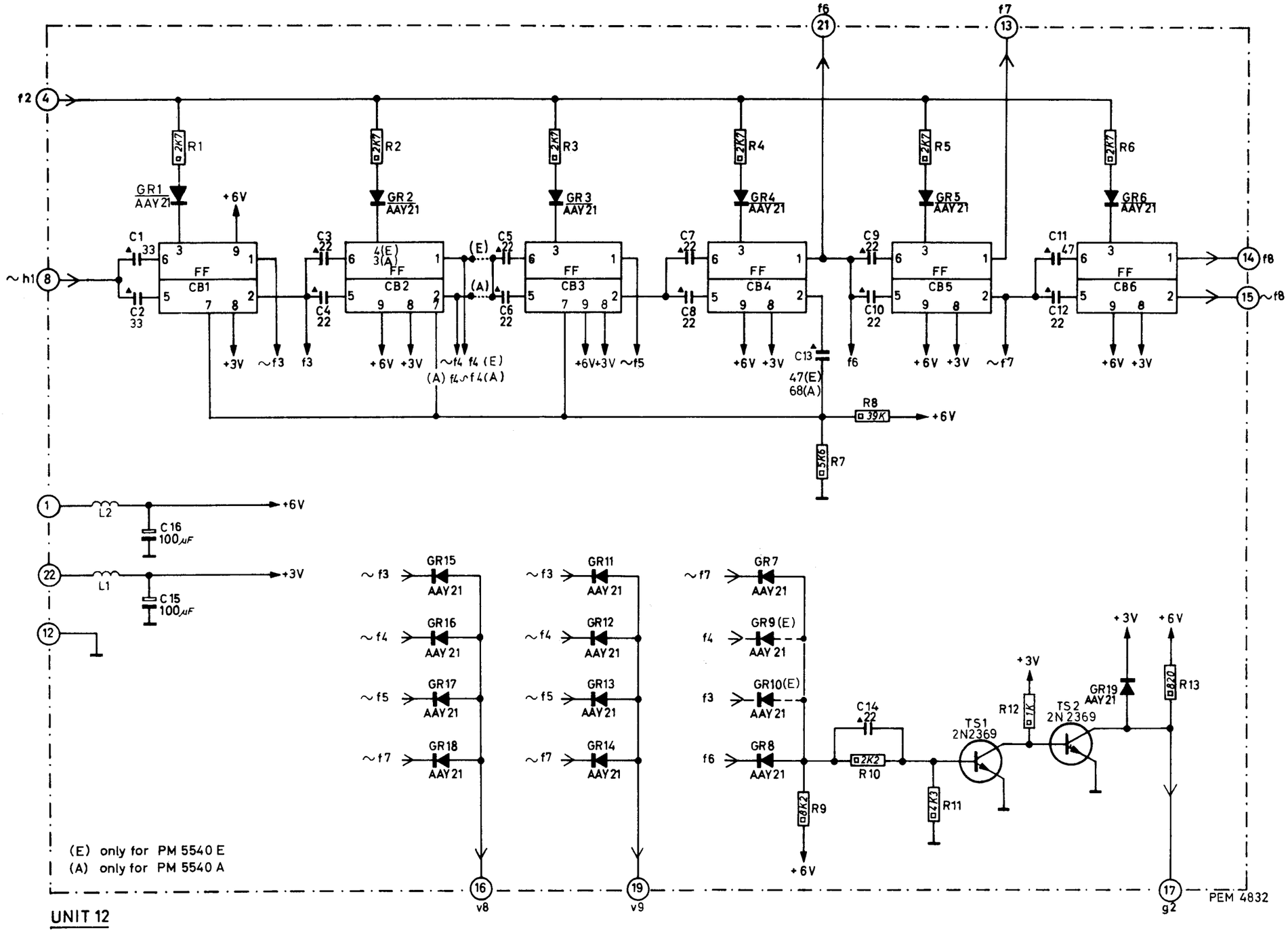


Fig. XVIII-6 Circuit diagram, vertical divider, Unit 12

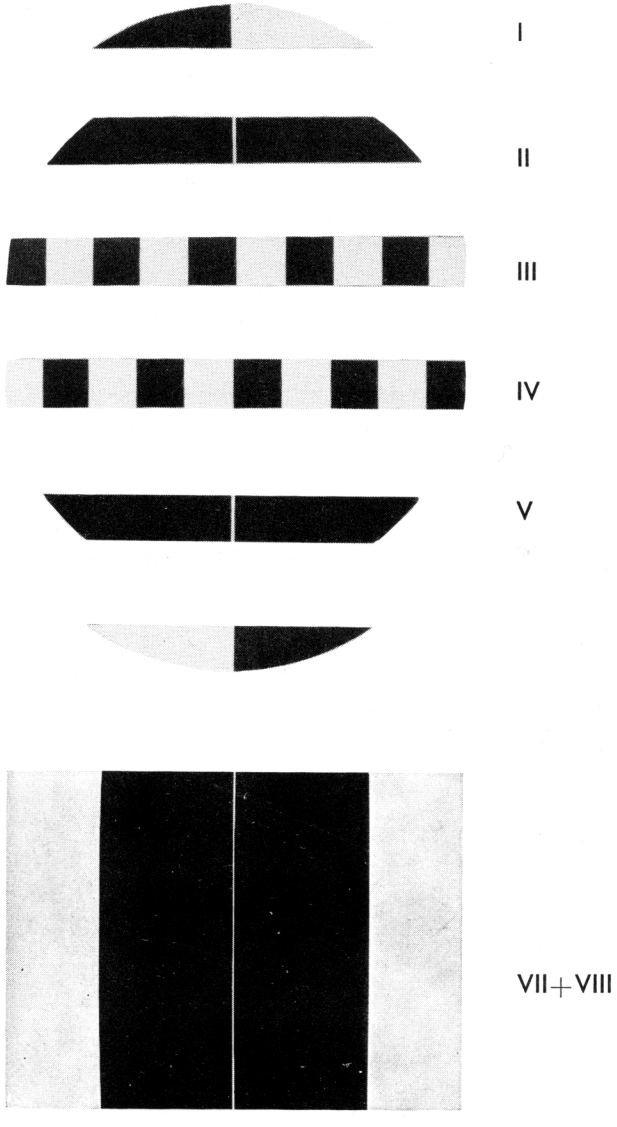
XIX Unit 13

The black and white steps

This circuit, formed by 10 AND-gates (I . . . X) and 10 OR-gates (BAY38), supplies the information to produce two complete test patterns as well as parts of the circle-area (see Fig. XIX-1).
The circuit also contains the one-shot generator TS1, which supplies the needle pulse "k8". The pulse time (200 ns) depends on the RC time of C3/R11.
By depressing the push-buttons (front of instrument, see connections terminal blocks) the AND-gates are supplied with +6 V: P1, P3, P4 and P6. The combined pulses in these gates are applied via the OR-gates, to amplifier TS2. The resulting pulse "d1" is used in the Cross-bar gate (unit 15).
The thin white vertical line in the lower black part of the circle can be removed by interrupting diodes GR20 and GR21.
The unbroken black fields then obtained can be used for inserting text from e.g. a camera.

Checking and adjusting
Measuring equipment:
Oscilloscope: e.g. PHILIPS PM 3330.

Needle pulse "k8"
Depress SK4 "BL/WH. STEP".
Connect oscilloscope to the junction of GR28 and GR 29. The needle pulse width "k8" should be 200 ns, + or – 10 ns.
If not, select another value for C3 (12 pF – 22 pF).



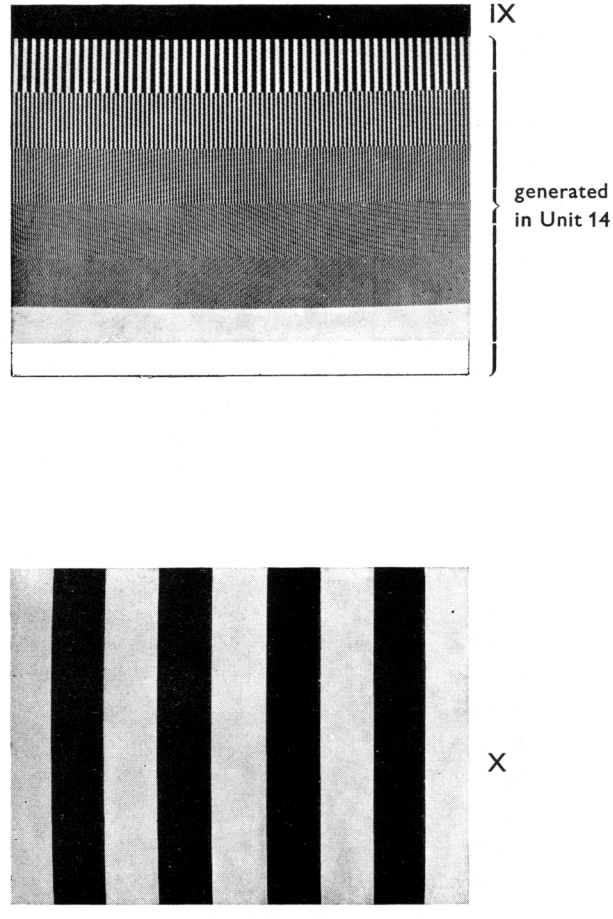
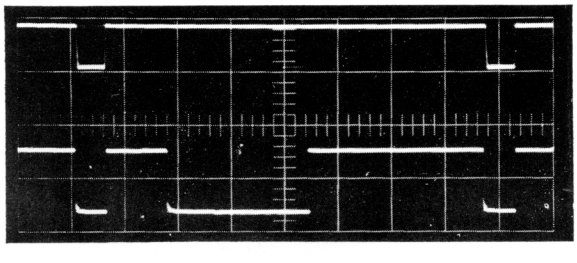
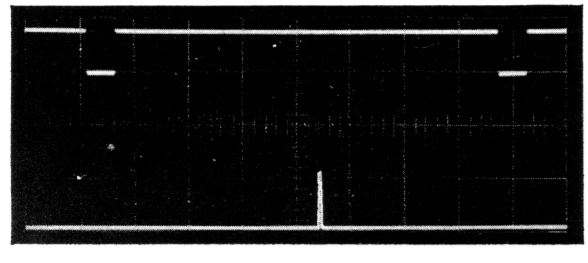


Fig. XIX-1 Parts of testpattern



~ k3
2 V/cm 8 µs/cm
reference: line sync.



k8
5 V/cm 8 *s/cm
reference: line sync.

Fig. XIX-2 Oscillograms, Unit 13

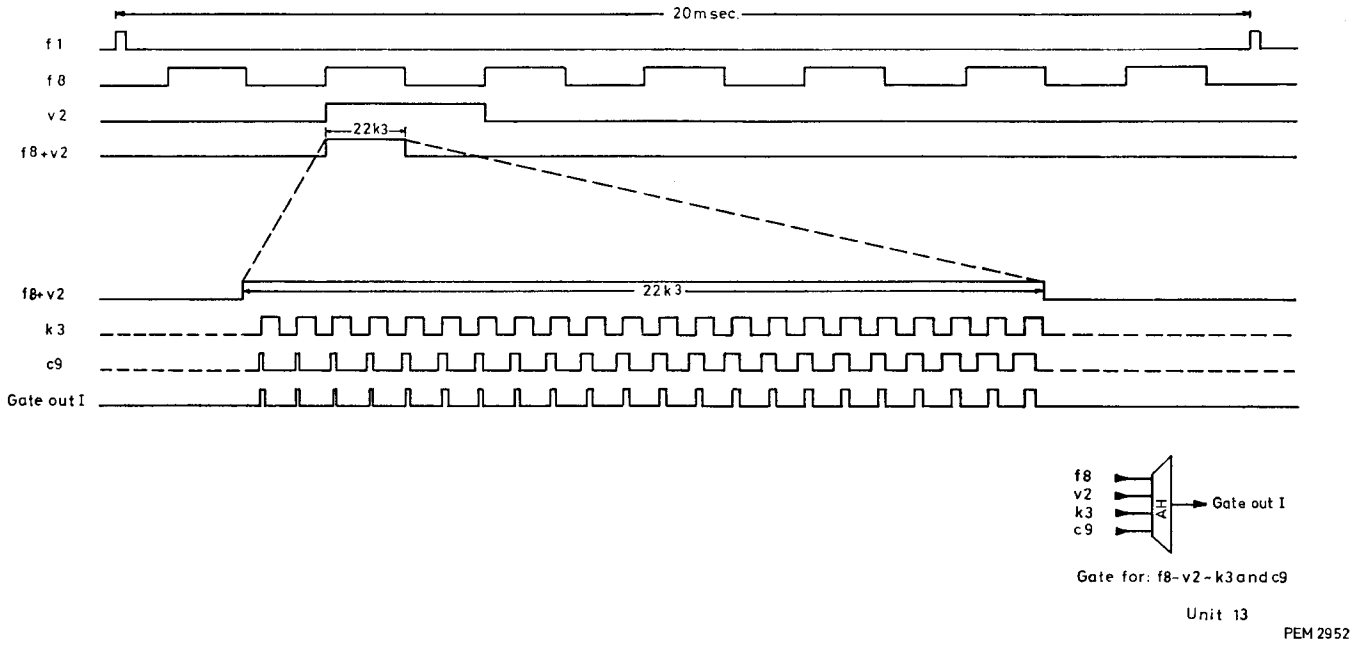


Fig. XIX-3 Pulse diagram of gate I

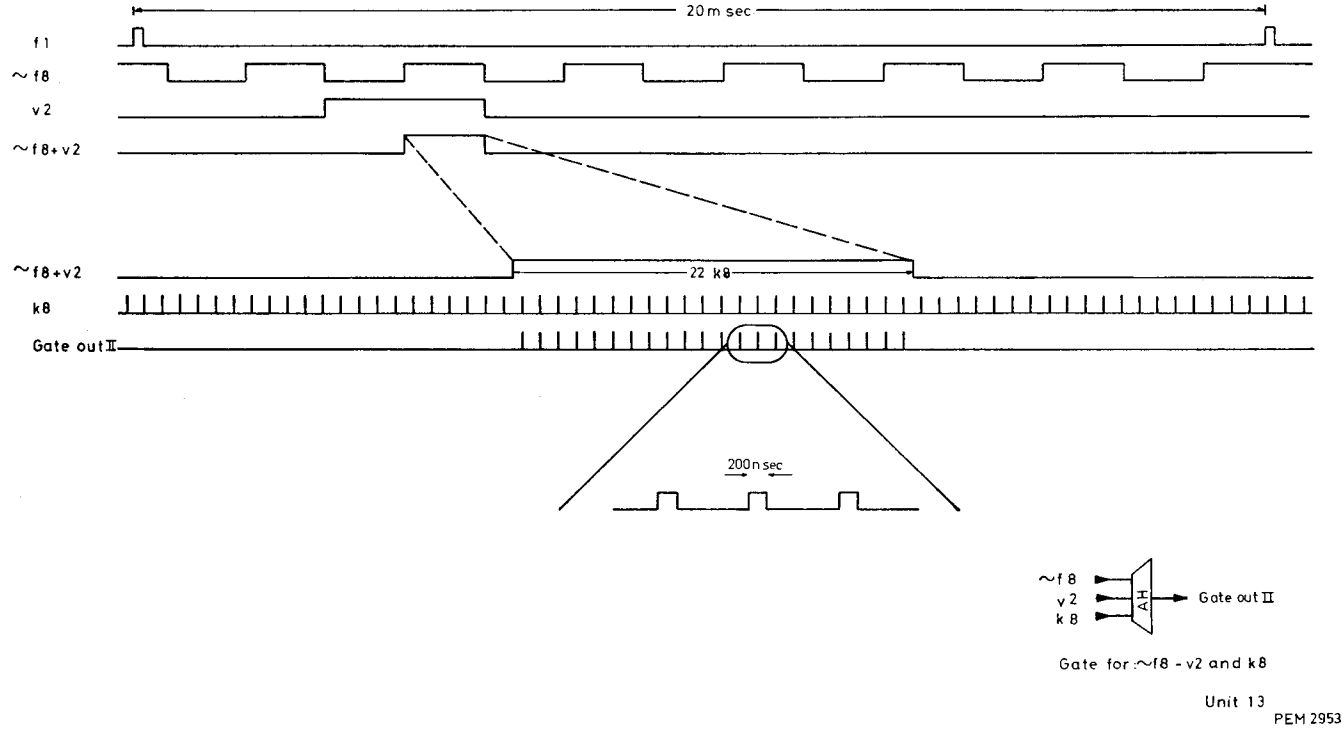


Fig. XIX-4 Pulse diagram of gate II

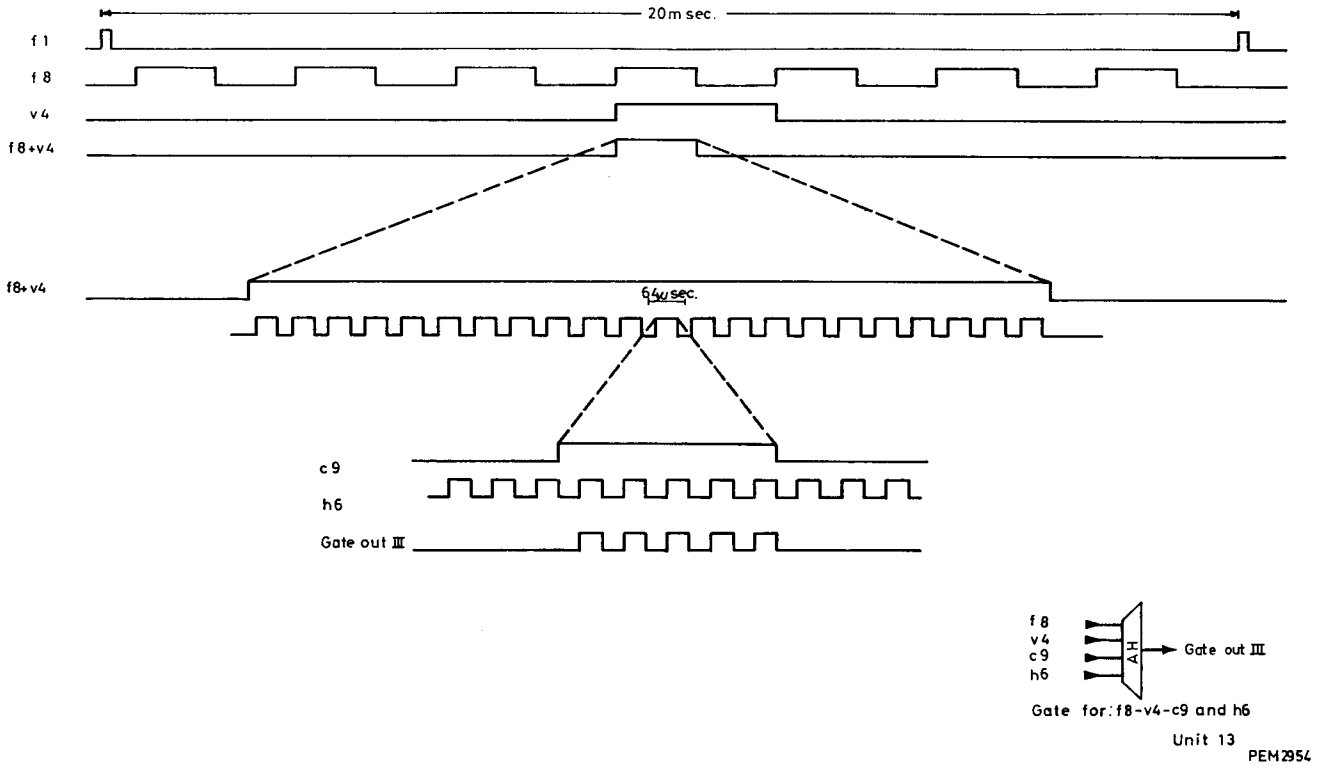


Fig. XIX-5 Pulse diagram of gate III

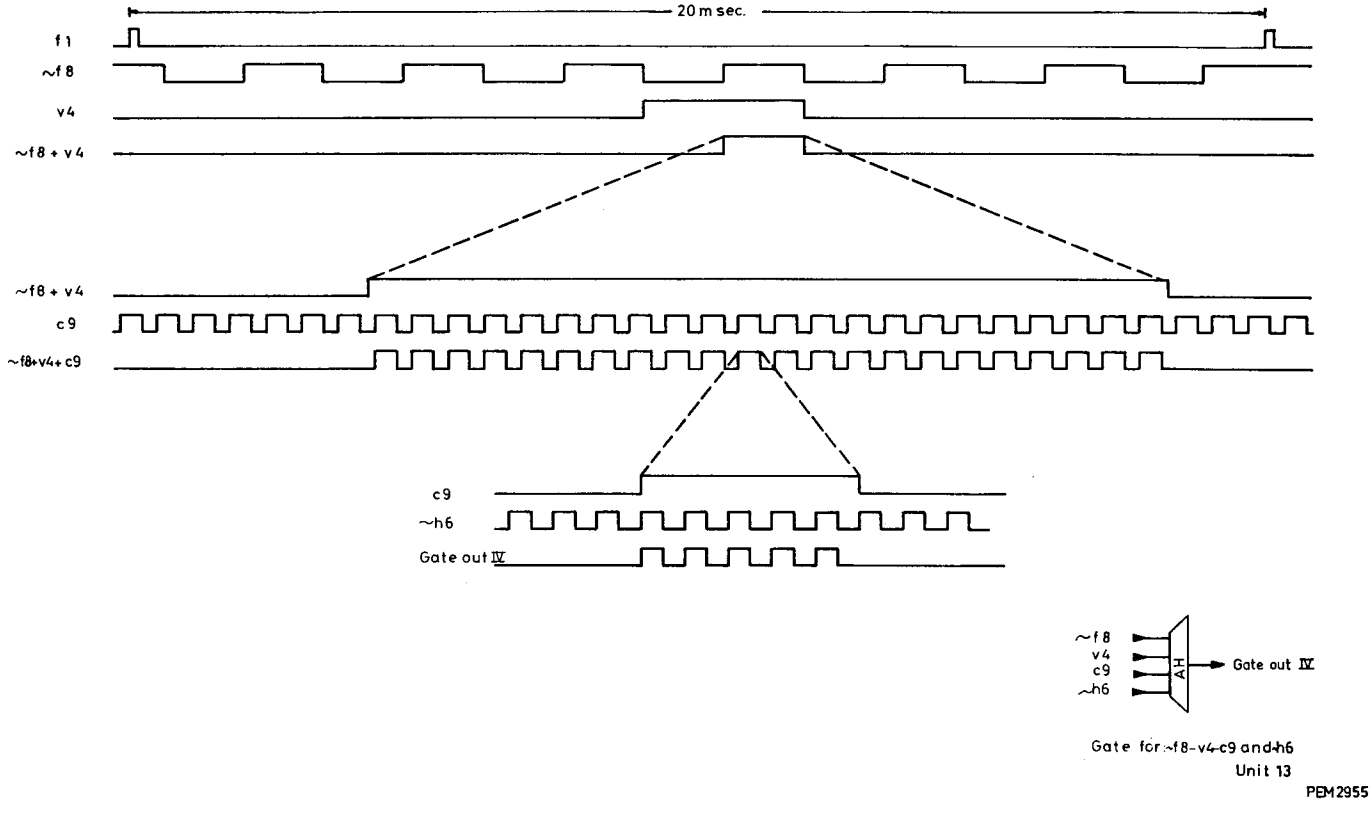


Fig. XIX-6 Pulse diagram of gate IV

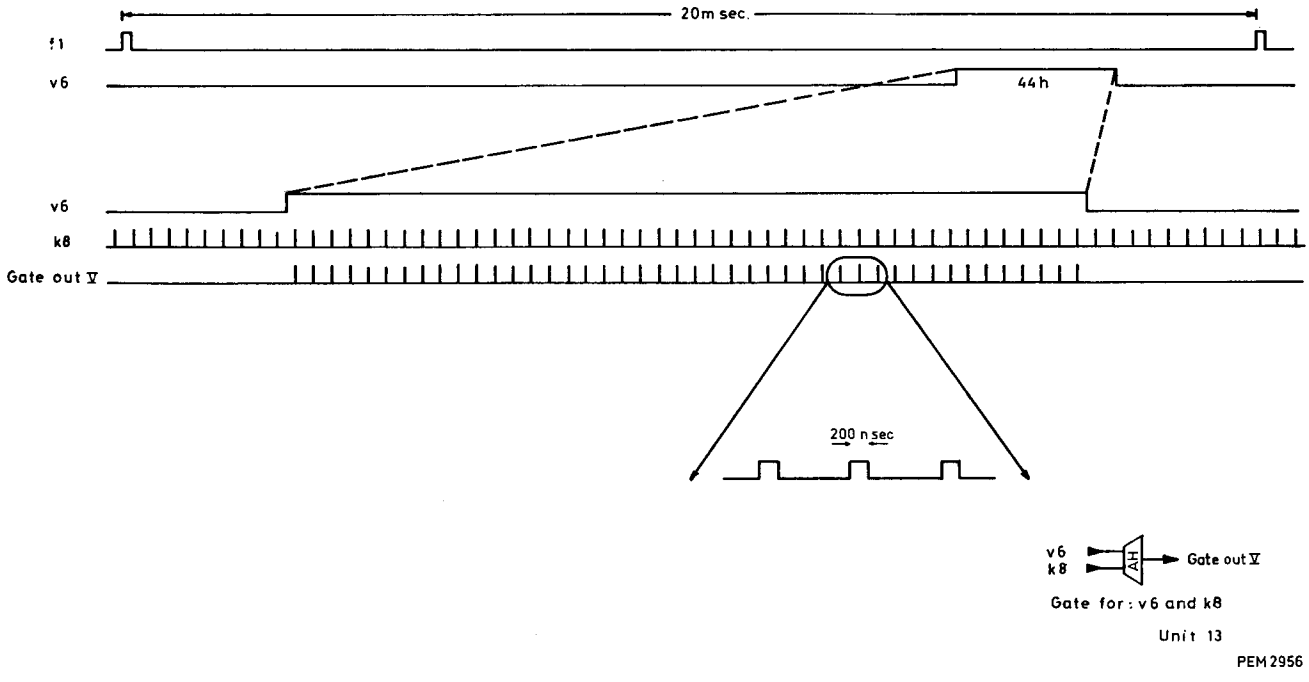


Fig. XIX-7 Pulse diagram of gate V

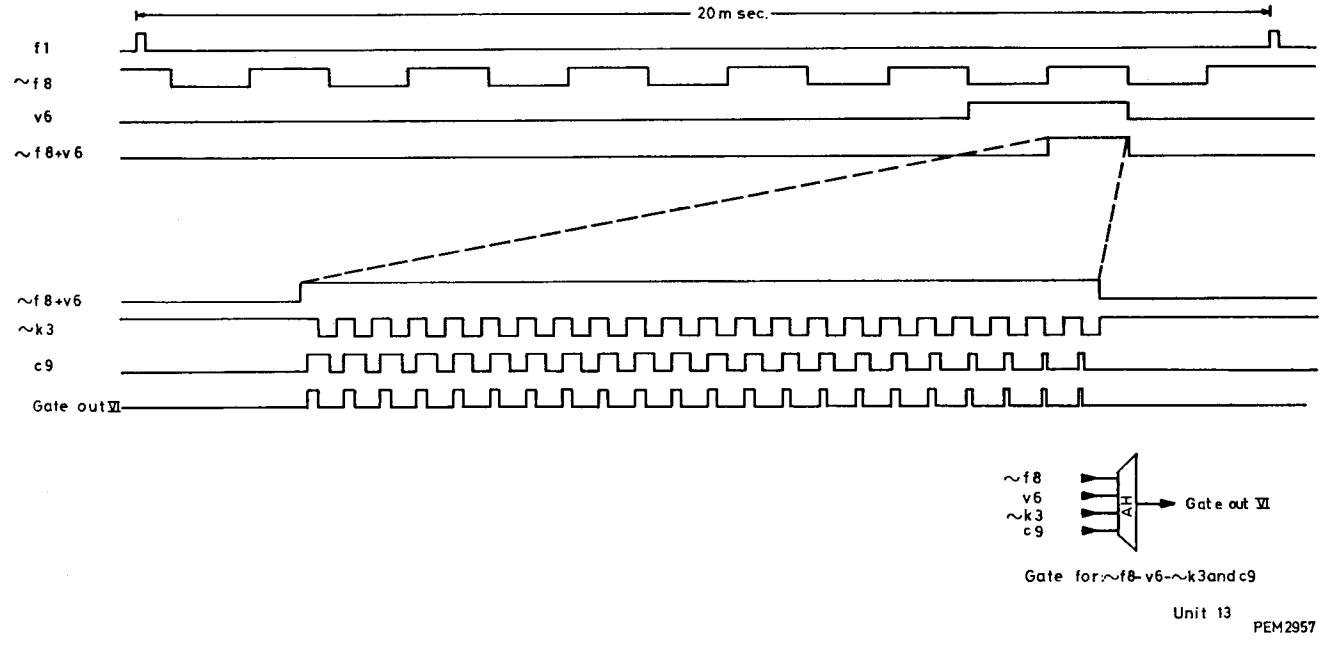


Fig. XIX-8 Pulse diagram of gate VI

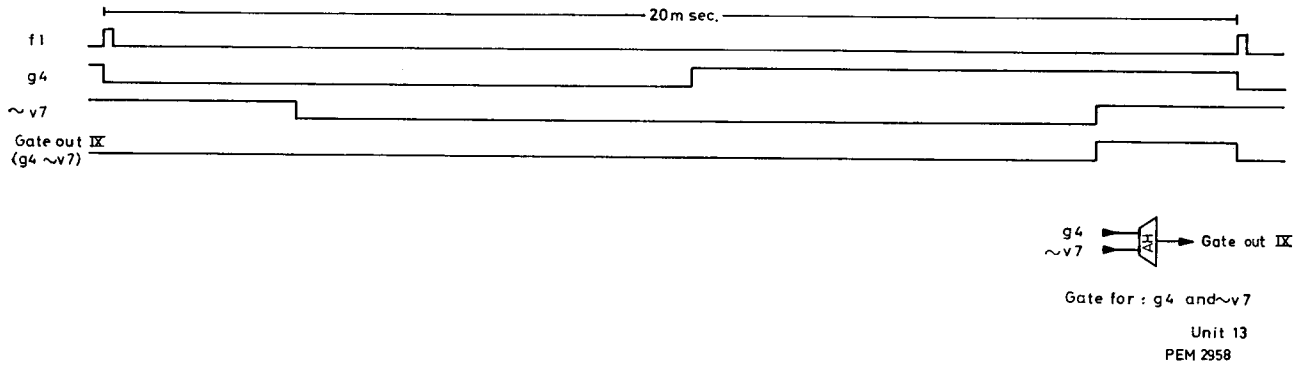


Fig. XIX-9 Pulse diagram of gate IX

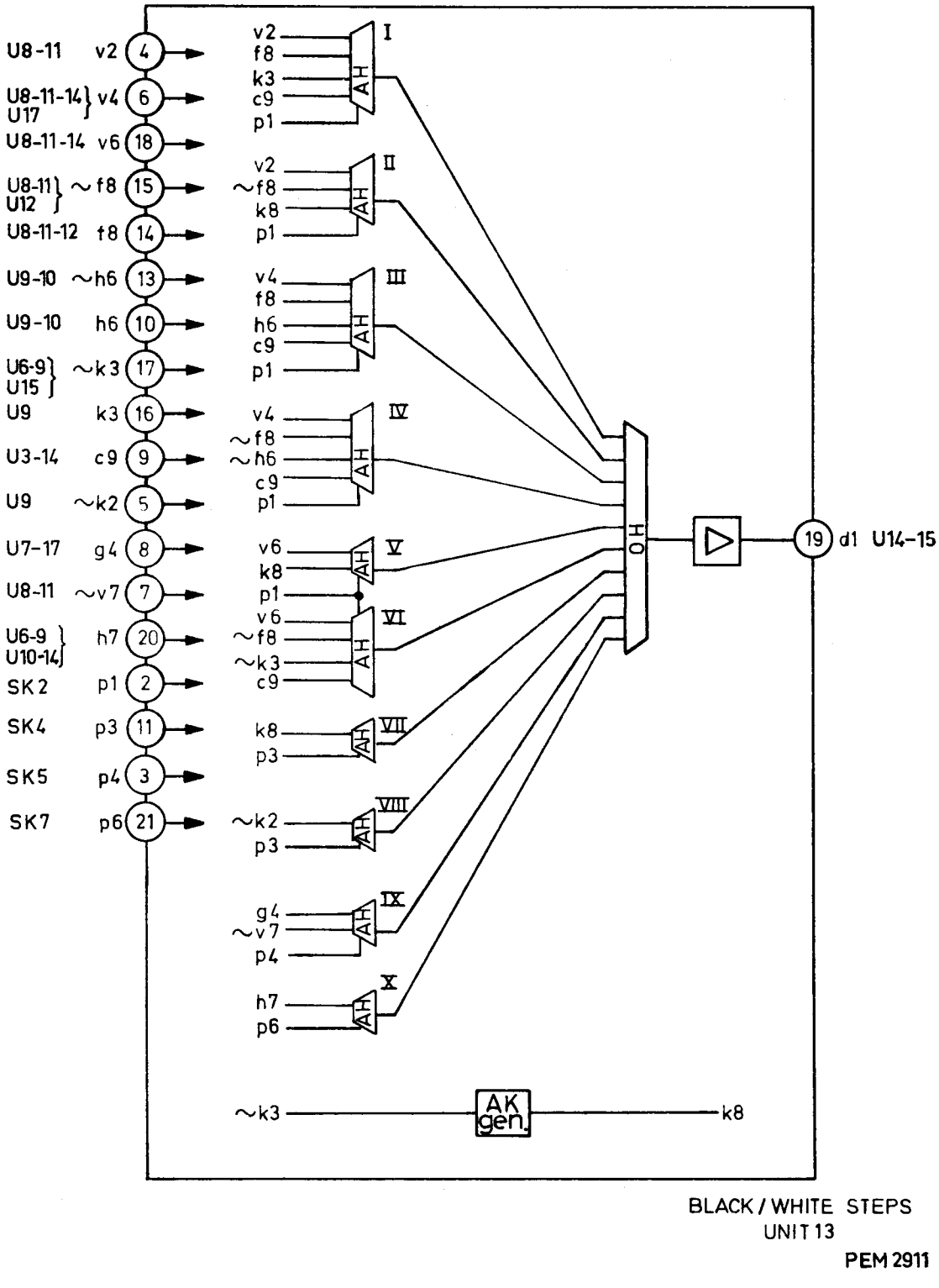


Fig. XIX-10 Block diagram, black/white steps, Unit 13

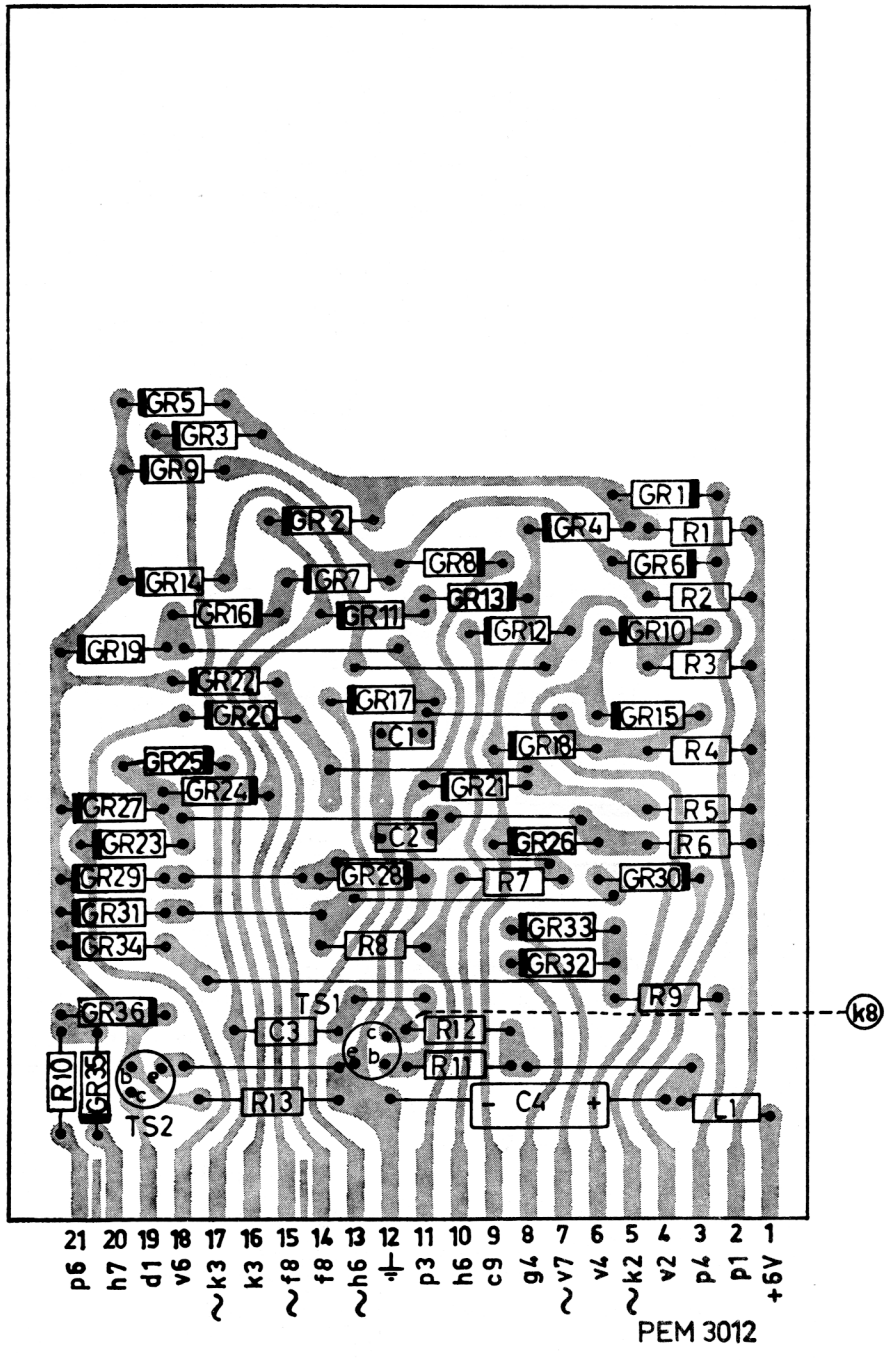


Fig. XIX-11 Printed wiring board, black/white steps, Unit 13

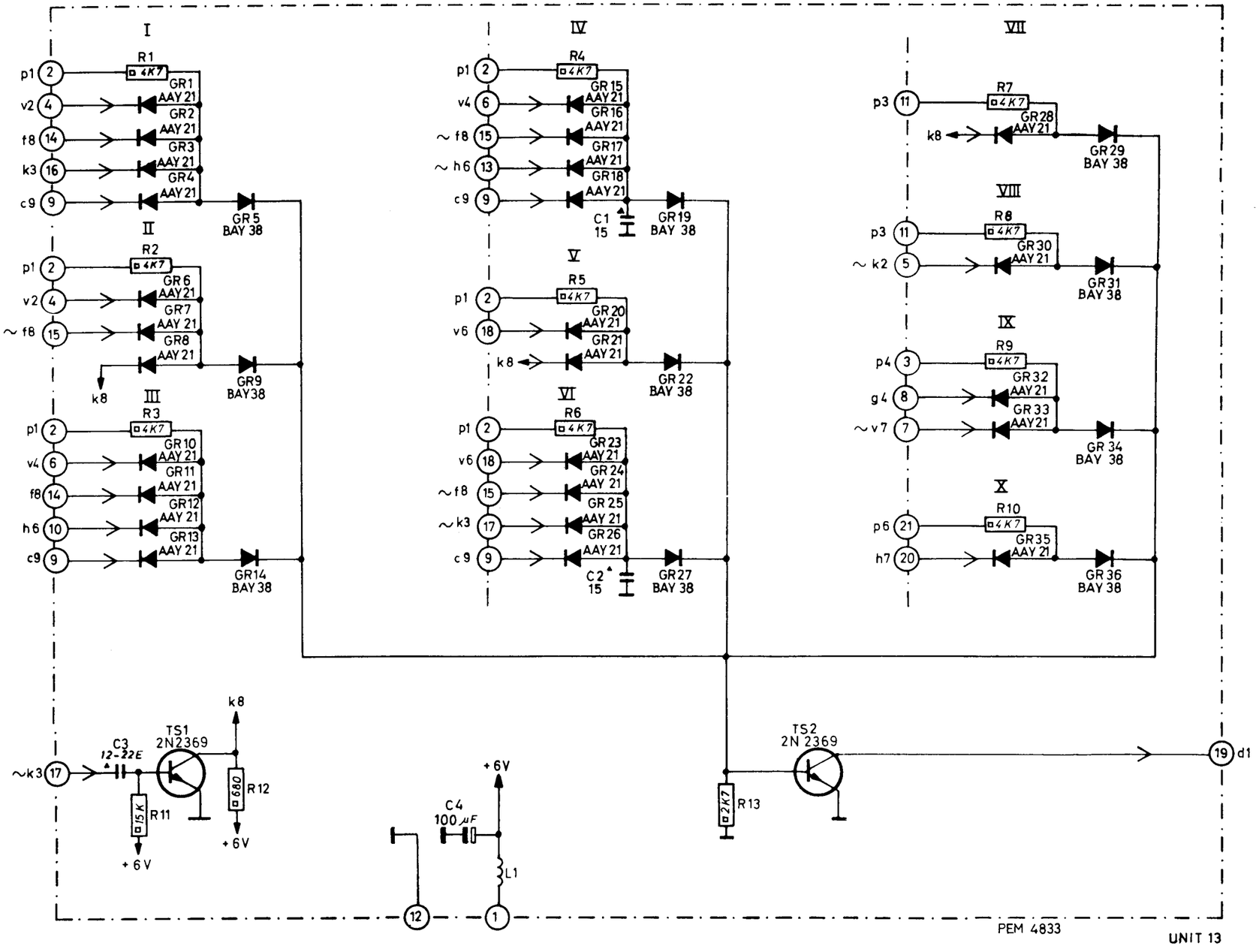


Fig. XIX-12 Circuit diagram, black/white steps, Unit 13

XX Unit 14

The linear gate

This unit contains the following circuits:
1. Definition lines generator
2. Horizontal step generator
3. Vertical step generator
4. Staircase amplifier

Generator for the definition lines

This generator (a multivibrator consisting of TS18 and TS20), is operating in the frequency range of 0.8-4.8 MHz. The frequency is determined by the voltage across the speed-up capacitors C8 and C9 and is controlled by TS15 or TS16. Frequency drift is compensated by TS17 and TS19 (diode connected) which are inserted in the collector circuit of TS18 and TS20 respectively. By depressing push-button SK2 or SK5 (at the front of the instrument), TS16 or TS15 respectively, are supplied with a level P1 or P4 respectively thus passing a horizontal or vertical staircase signal respectively to the generator. The signal which is applied, via TS14, to TS16 is a, horizontal staircase signal, while the signal applied to TS15 via TS13, is a vertical staircase signal. To ensure the multivibrator always starts in the same phase (beginning with white), start and stop are controlled by the blanking pulse ("a1") which is applied, via TS21, to the base of TS17 and the collectors of TS15 and TS16. The output signal of the multivibrator ("d2") is, via the AND-OR gates GR19 . . . GR25 and the amplifier TS22, applied to the Cross-bar gate (unit 15).

Generator for the horizontal staircase signal

This signal which is produced by dividing the +6 V in five different steps is used to control the definition lines generator in horizontal direction. The dividers are formed by R17, R18 and R25//R26 solely, or together with resistors R15, R16, R19 . . . R24, switched in parallel to R25//R26 by transistors TS1 . . . TS4.
First step is produced by the divider R17, R18 and R25//R26.
Second step:
by the first divider in parallel with R21//R22, TS3 being driven into saturation by the "h9" pulse.
Third step:
by the first and second divider in parallel with R23// R24, TS4 is also driven into saturation by the "h8", "h9" and "k1" pulses.
Fourth step:
TS2 is also driven into saturation connecting R19//R20 in parallel as well.
Fifth step:
TS1 is also driven into saturation connecting R15//R16 in parallel also.
Resistors R16, R20, R22, R24 and R26 are selected to obtain the correct level for each individual step.

Generator for the vertical step signal

This signal is produced by dividing the +6 V across R27 and R36//R37 solely, or in parallel with the collector resistors R28 . . . R35 of the transistors TS5 . . . TS8.
First step is produced by divider R27 and R36//R37.
Second step:
by the first divider in parallel with R34//R35. TS8 is driven into saturation by the "v6" pulse.
Third step:
by the first divider in parallel with R32//R33. TS7 is driven into saturation by the "v5" pulse.
Fourth step:
by the first divider in parallel with R30//R31. TS6 is driven into saturation by the "v4" pulse
Fifth step:
by the first divider in parallel with R28//R29. TS5 is driven into saturation by the "v3" pulse.
Resistors R29, R31, R33 R35 are selected to obtain the correct level for each individual step.

Amplifier for the staircase signal

The horizontal step signal is also used to produce the gradation steps inside the circle area.
The horizontal step level (3-5.5 V) is reduced (0-3 V) by TS9 and TS12. The collector level of TS12 is adjusted to zero by R41 (without signal). By depressing push-button SK1, the AND-gate GR12-GR13 is activated by level P1, while TS10 (a constant current

generator) is driven into saturation. During saturation of TS10, TS9 and TS11 are cut-off and the step signal is blocked, when TS10 is driven into cut-off by the "v5" and "c9" pulses, TS9 and TS11 are conducting and the step signal is passed on to the Cross-bar gate (unit 15).

Checking and adjusting
Measuring equipment:
Oscilloscope: e.g. PHILIPS PM 3330.
With dual-trace-Y amplifier: e.g. PHILIPS PM 3342.

A. Definition lines of the complete pattern
Depress Sk2 "COMPL. PATTERN".
Remove unit 5 "MEMORY".
Connect the A amplifier of the oscilloscope to BU8 "VIDEO II OUT", and the B amplifier to the base of TS14 (Junction R17-R18).
Trigger externally with the "v3" pulse (terminal 20).
The oscillogram should be as shown in figure XX-1a.
Select one step of the staircase.

1. Frequency of 0.8 MHz (Fig. XX-1b)
Check that there are 4.5 pulses on this step.
If not, select another value for R26 (33 kΩ . . . 100 kΩ).

2. Frequency of 1.8 MHz (Fig. XX-1c)
Check that there are 11 pulses on this step.
If not, select another value for R22 (4.7 kΩ . . . 15 kΩ).

3. Frequency of 2.8 MHz (Fig. XX-1d)
Check that there are 17 pulses on this step.
If not, select another value for R24 (2.7 kΩ . . . 10 kΩ).

4. Freqency of 3.8 MHz (Fig. XX-1e)
Check that there are 23 pulses on this step.
If not, select another value for R20 (2.7 kΩ . . . 10 kΩ).

5. Frequency of 4.8 MHz)Fig. XX-1f)
Check that there are 29 pulses on this step.
If not, select another value for R16 (1 kΩ . . . 2.7 kΩ).

B. Definition lines
Depress Sk5 "DEF. LINES".
Remove unit 5 "MEMORY".
Connect the A amplifier of the oscilloscope to BU5 "VIDEO I OUT" and the B amplifier to the base of TS14 (Junction R17-R18).
Trigger externally as described for each section.
Select one step of the staircase.

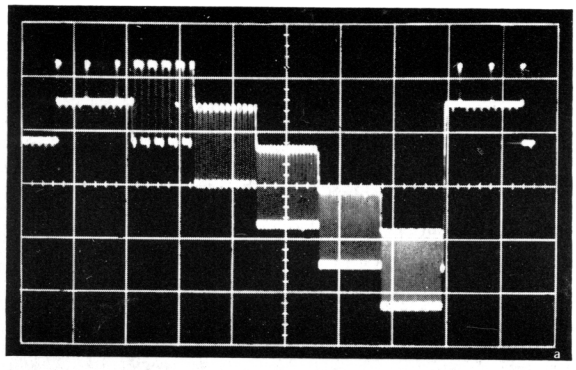
1. Frequency of 0.8 MHz (Fig. XX-1g)
Trigger with the "v2" pulse (terminal 4 of unit 11).
Check that there are 4.5 pulses on this step.
If not, select another value for R37 (10 kΩ . . . 68 kΩ).

2. Frequency of 1.8 MHz (Fig. XX-1h)
Trigger with the "v3" pulse (terminal 20 of unit 14).
Check that there are 11 pulses on this step.
If not, select another value for R29 (4.7 kΩ . . . 22 kΩ).

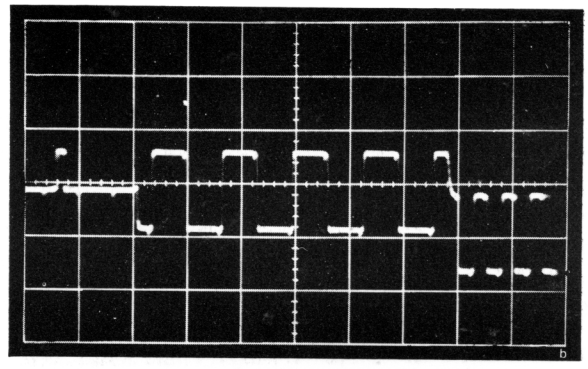
3. Frequency of 2.8 MHz (Fig. XX-1k)
Trigger with the "v4" pulse (terminal 6 of unit 14).
Check that there are 17 pulses on this step.
If not, select another value for R31 (2.2 kΩ . . . 6.8 kΩ).

4. Frequency of 3.8 MHz (Fig. XX-1l)
Trigger with the "v5" pulse (terminal 10 of unit 14).
Check that there are 23 pulses on this step.
If not, select another value for R33 (820 Ω . . . 2.2 kΩ).

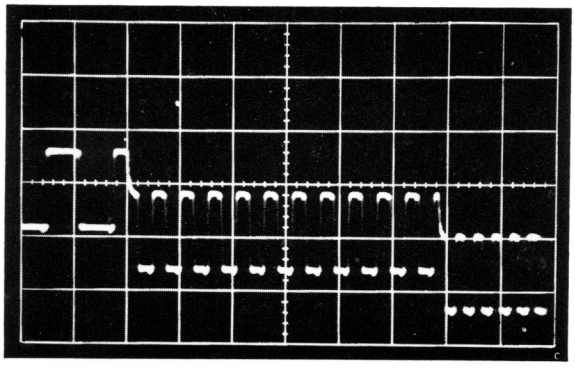
5. Frequency of 4.8 MHz (Fig. XX-1m)
Trigger with the "v6" pulse (terminal 18 of unit 14).
Check that there are 29 pulses on this step.
If not, select another value of R33 (1 kΩ . . . 3.9 kΩ).



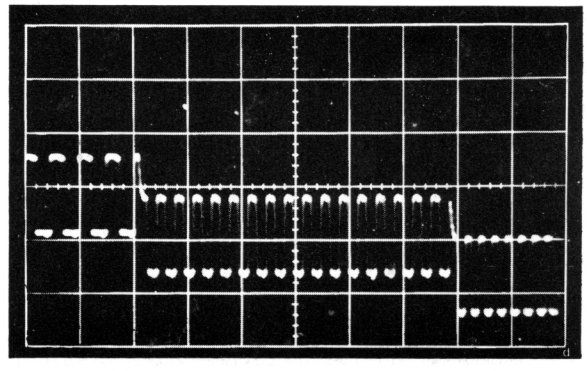
a
Complete pattern



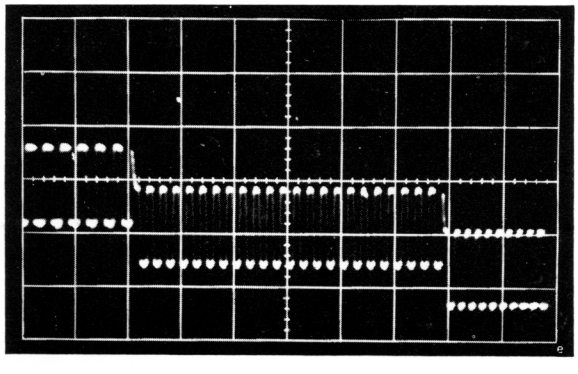
b
0.8 MHz



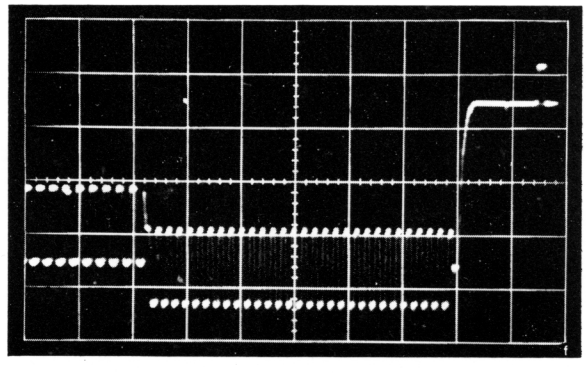
c
1.8 MHz



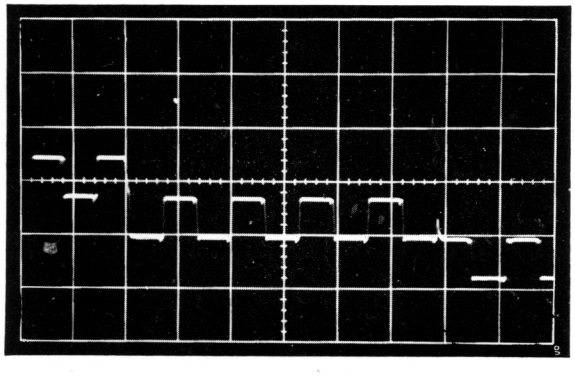
d
2.8 MHz



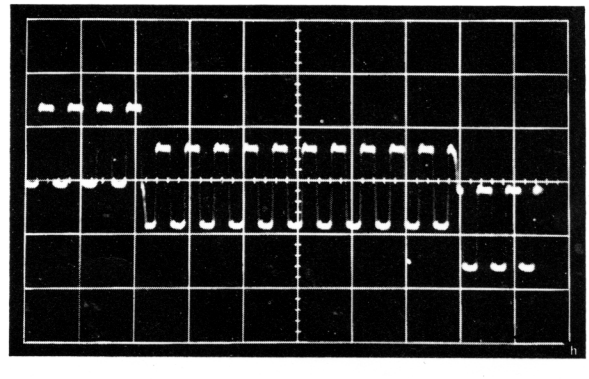
e
3.8 MHz



f
4.8 MHz

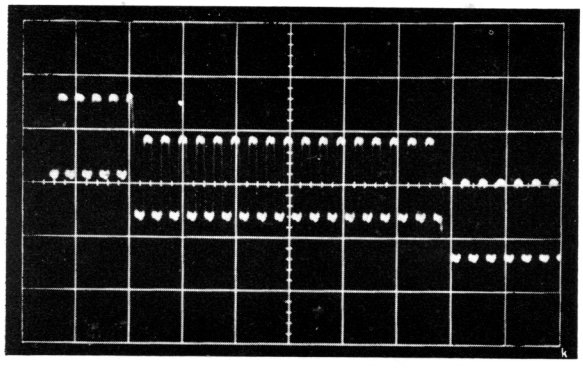


g
0.8 MHz

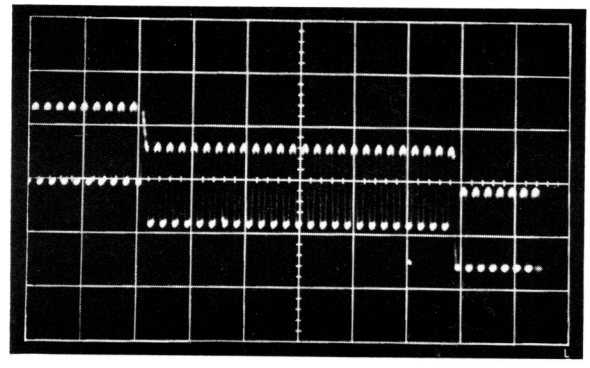


h
1.8 MHz

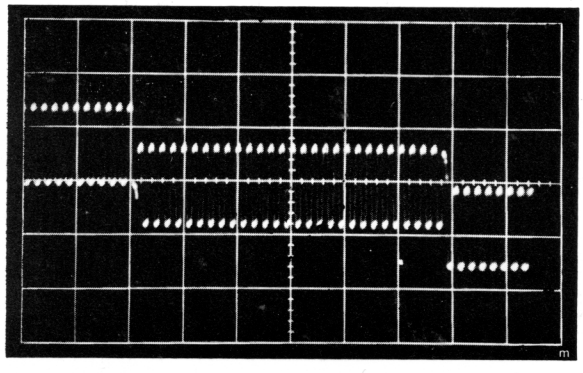
Fig. XX-1 Oscillograms, Unit 14



k
2.8 MHz



l
3.8 MHz



m
4.8 MHz

Fig. XX-1 Oscillograms, Unit 14

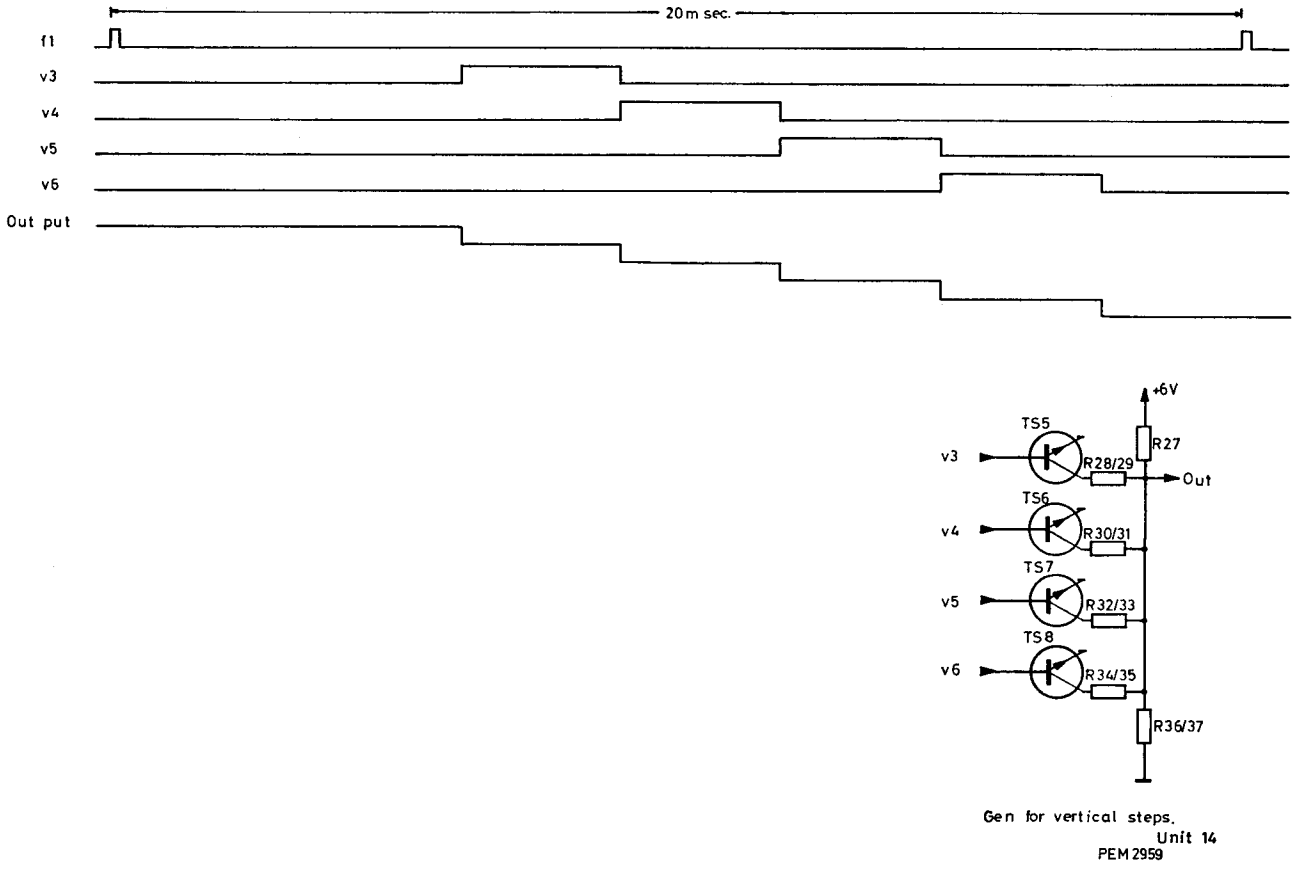


Fig. XX-2 Pulse diagrams for vertical steps

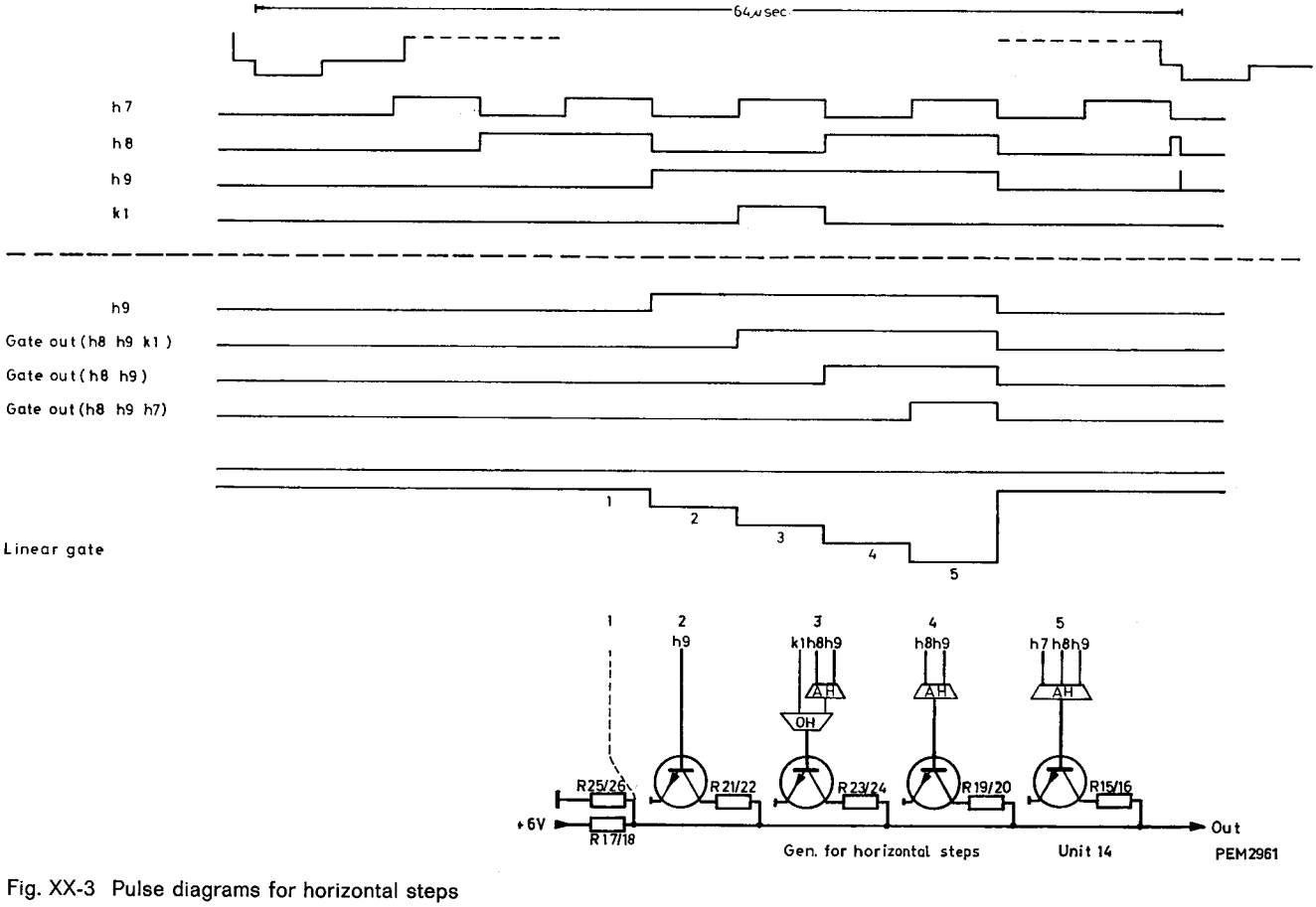


Fig. XX-3 Pulse diagrams for horizontal steps

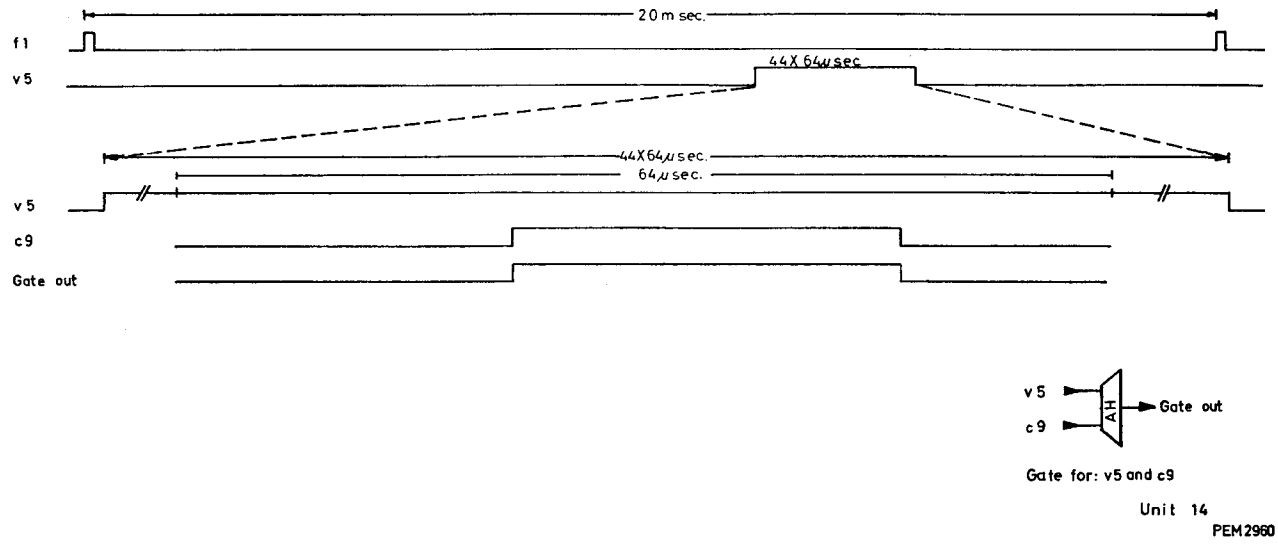


Fig. XX-4 Pulse diagrams for "v5" and "c9"

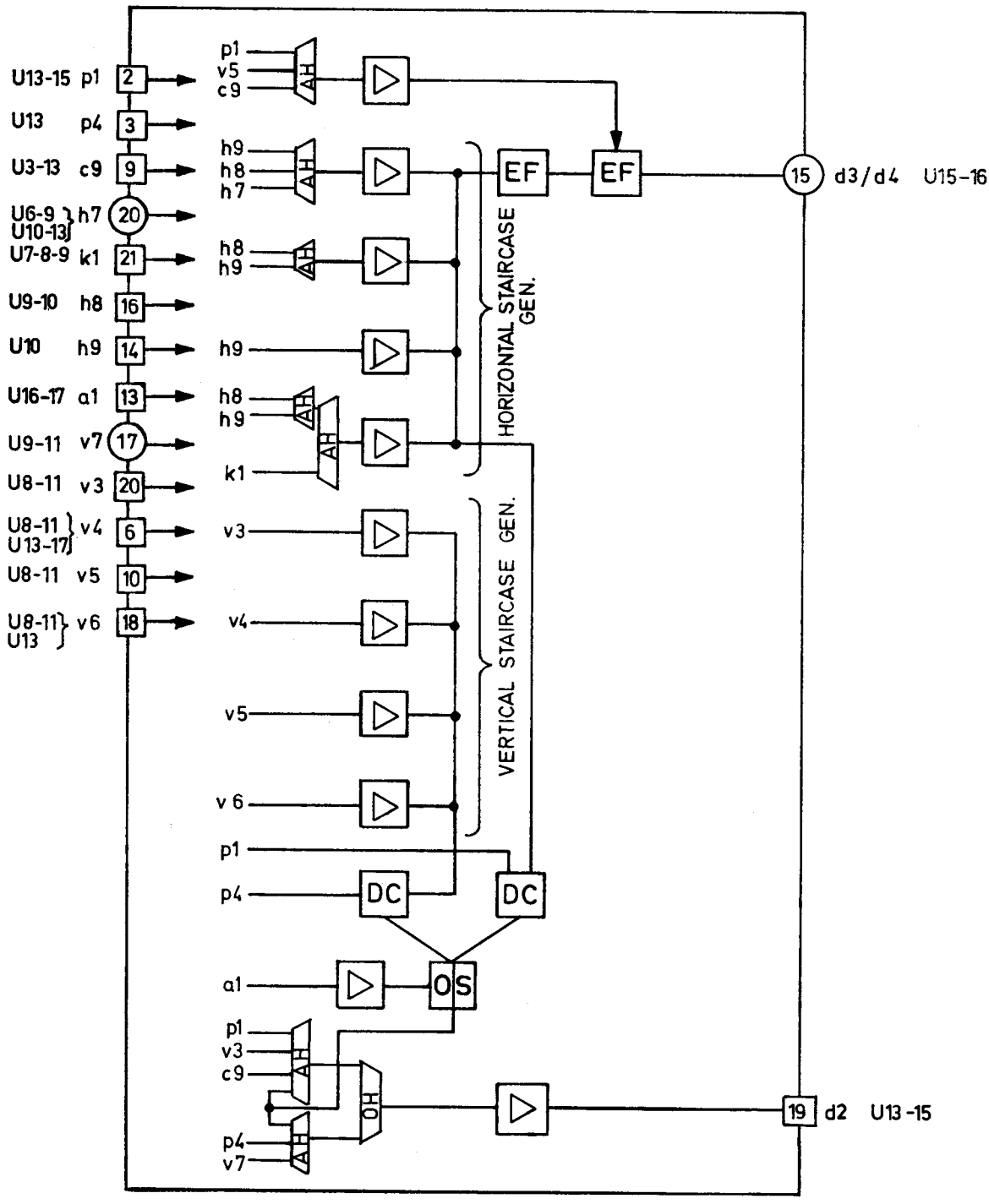


Fig. XX-5 Block-diagram, linear gate, Unit 14

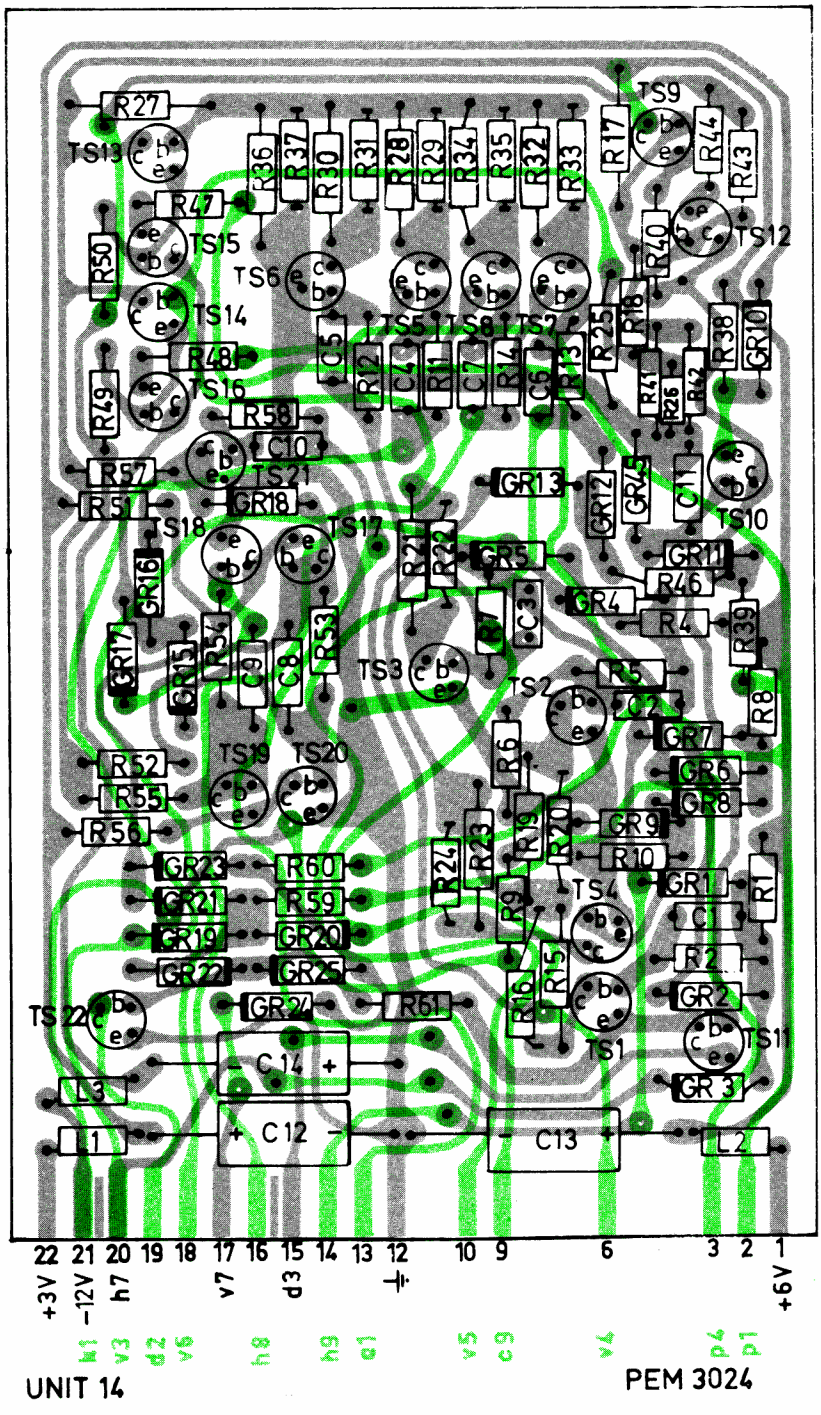
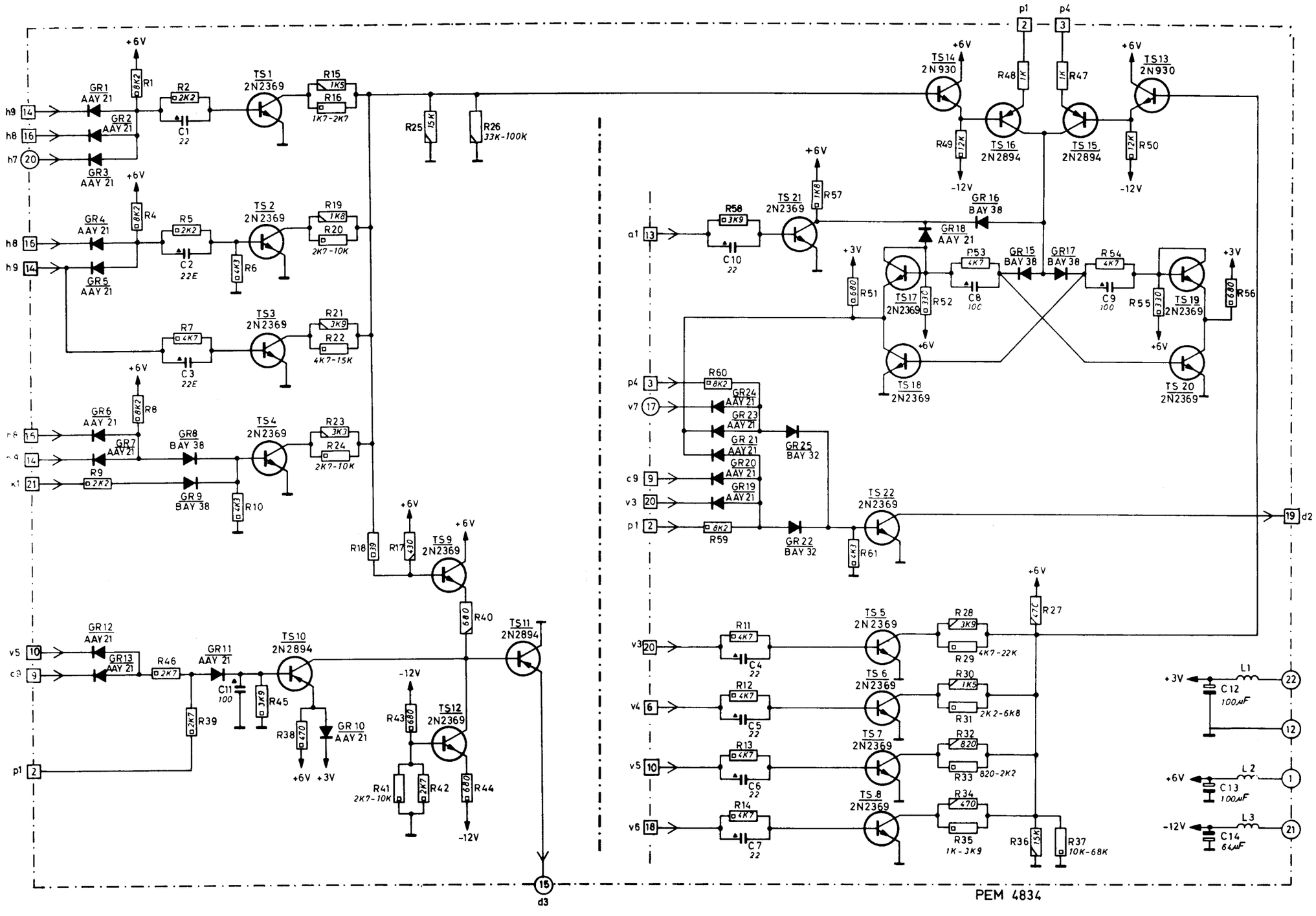


Fig. XX-6 Printed wiring board, linear gate, Unit 14



From version /06 the following is modified:
— GR 18 is removed
— R17 has become 390 Ω
— R18 has become 82 Ω
— Collector of TS17 is connected to the collector of TS21

Fig. XX-7 Circuit diagram, linear gate, Unit 14

XXI Unit 15

The cross-bar gate

The cross-bar gate produces the grey background, the horizontal and vertical white lines as well as the black-white squares at the borders. In this section, these patterns are combined with the circular pattern to form the complete testpattern.

Generator for the vertical white lines
(I + II in Fig. XXI-2)

The vertical white lines are controlled by the AND-gates GR14 . . . GR17. Gate GR16 . . . GR17 controls the first white line, while GR14 . . . GR15 control the other lines. The combined pulses from these gates are differentiated by R23, C6 and C7, driving TS6 into cut off for a time of 200 ns which is determined by the RC time of R23, C6 and C7.

Generator for the horizontal white lines
(VI in Fig. XXI-2)

This generator consists of gates GR23 in this unit and GR15 . . . GR18 in unit 12 (producing the "v8" pulse).
The "v8" pulse passes through OR-gate GR22 and is determined by the "∿ v1" pulse.

Generator for the black/white squares
(IV + V in Fig. XXI-2)

The black/white squares at top and bottom of the pattern are produced, via AND-gates GR25 . . . GR26 and GR28 . . . GR29 by the "k4" and "h5" pulses which are combined with the "v1" pulses.
The combined signals ("∿ h4", "∿ k3", "k4" and "∿ k4" control TS7 via one shot TS6.
The squares at left and right hand side are produced, via AND-gate GR31 . . . GR32, by the "k4" and "∿ g3" pulses. Because of the uniform size of the black/white squares, there would remain little black-squares in the corners of the pattern. Due to the action of the "k4" and "v1" pulses however these squares are also white (see Fig. XXI-1).
The generated signals are combined in the OR-gate GR22, GR24, GR27 and GR30 and control TS8. Since TS7 and TS8 are in parallel, these signals are mixed and applied to TS3.

The currents through TS7 and TS8 are controlled, via TS9 and OR-gate GR19 . . . GR20, by the pulse "∿ c9" and P1 or P2 depending on which push-button (SK2 or SK3) is depressed. If SK3 (P2) is depressed, the "∿ c9" pulse will be suppressed because AND-gate GR18 has not level P1 and the black circle III in Fig. XXI-2 will be disappeared. TS3 is not only supplied with the signals from TS7, but also with the black/white steps, definition lines, vertical bars and the contents of the circle (however without the gamma fields). The total signal is applied to the grey-generators.

Generator for the "∿ g3" pulse

The "∿ g3" pulse is produced in the binary divider CB1, which is set to zero for each field by the "f2" pulse, dividing the "f7" pulse.

Generator for the grey-background
(VII in Fig. XXI-2)

The generators, formed by TS4-TS5 and TS1 . . . TS2 are so connected that each produces one half of the white amplitude.
The complete video signal from TS3 is applied to TS4 . . . TS5 and also via OR-gate GR9 to TS1 . . . TS2. The output signals of TS1 . . . TS2 and TS4 . . . TS5 are added in GR12 so that the required black to white amplitude is obtained. Pulses "∿ v1" and "∿ k4" combined in GR2-GR3, control the grey-background of the "CROSS LINES" pattern, while pulses "∿ v1", "∿ k4" and "∿ c9", combined in GR4 . . . GR6, control the grey background of the "COMPL. PATTERN".
The AND-gates are opened by the levels "P2" and "P1" respectively by depressing the push-buttons SK3 or SK2 at the front of the instrument.
The "d3" signal (step signal from unit 14) is applied, via clamping diode GR13, to the adder also, to produce the gamma signal.
In the same way, signal "d4" (blank pattern or saw-tooth) is added.

Checking and adjusting
Measuring equipment:
Oscilloscope: e.g. PHILIPS PM 3330.

1. Amplitude level of the "d6" signal
Connect oscilloscope to the junction of GR12 and R7.
The amplitude level should be +3 V.
The signal should be approx. 1 V_{pp}.
If not, select another value for R34 (560 Ω – 5.6 kΩ).

2. Grey level of the "d6" signal
Connect oscilloscope to the junction of GR12 and R7.
The grey level should be 2.5 V.
If not, select another value for R35 (560 Ω – 5.6 kΩ).

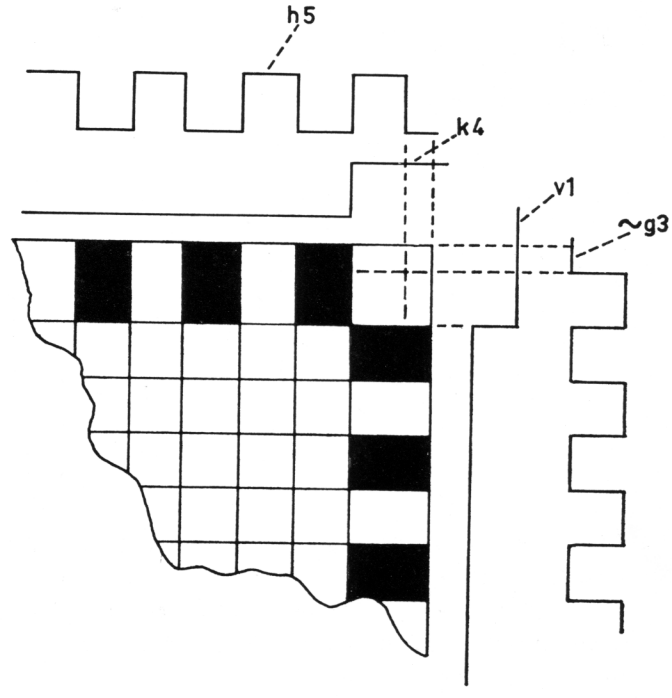


Fig. XXI-1 Influence of "k4" and "v1"

I = vertical lines
II = first vertical line
III = black circle
IV = black and white squares
V = black and white squares
VI = horizontal lines
VII = grey background

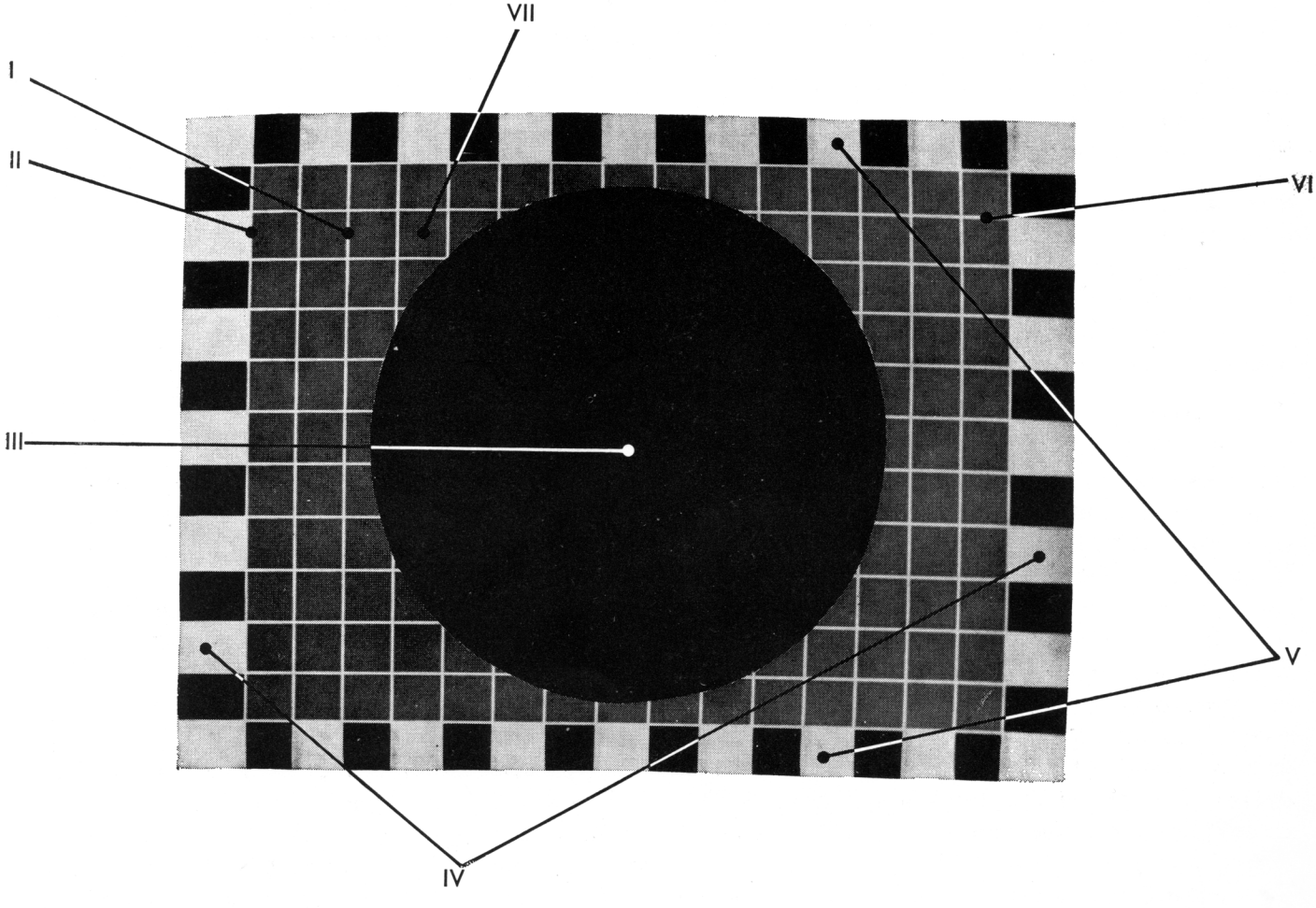


Fig. XXI-2 Test pattern

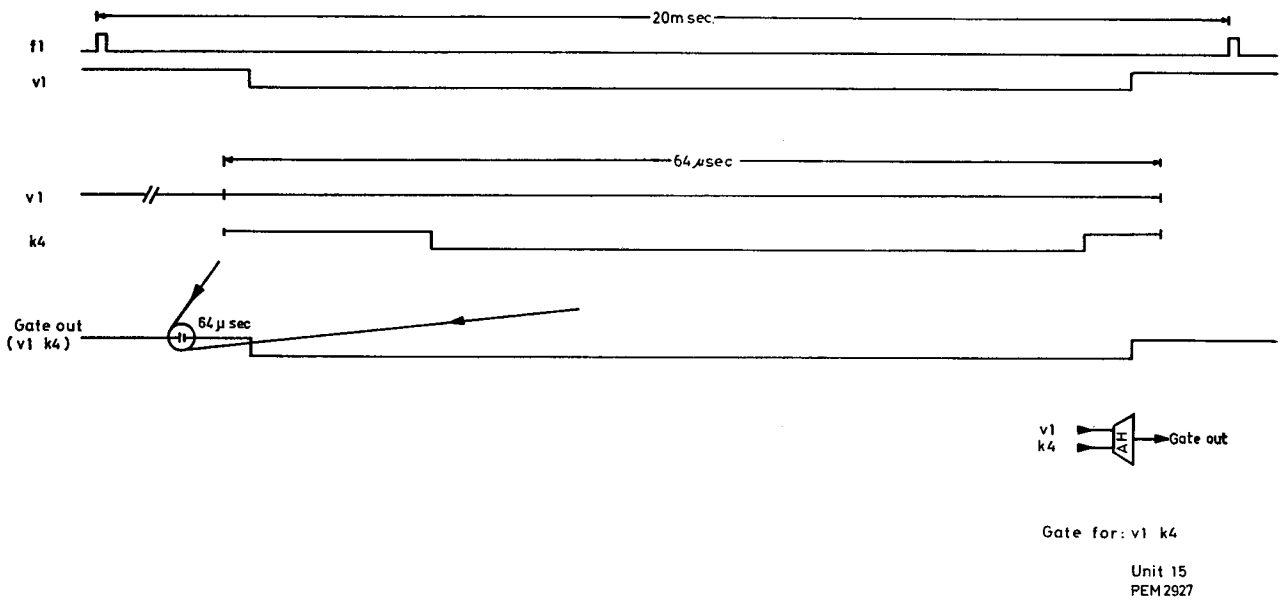


Fig. XXI-3 Pulse diagrams for "k4" and "v1"

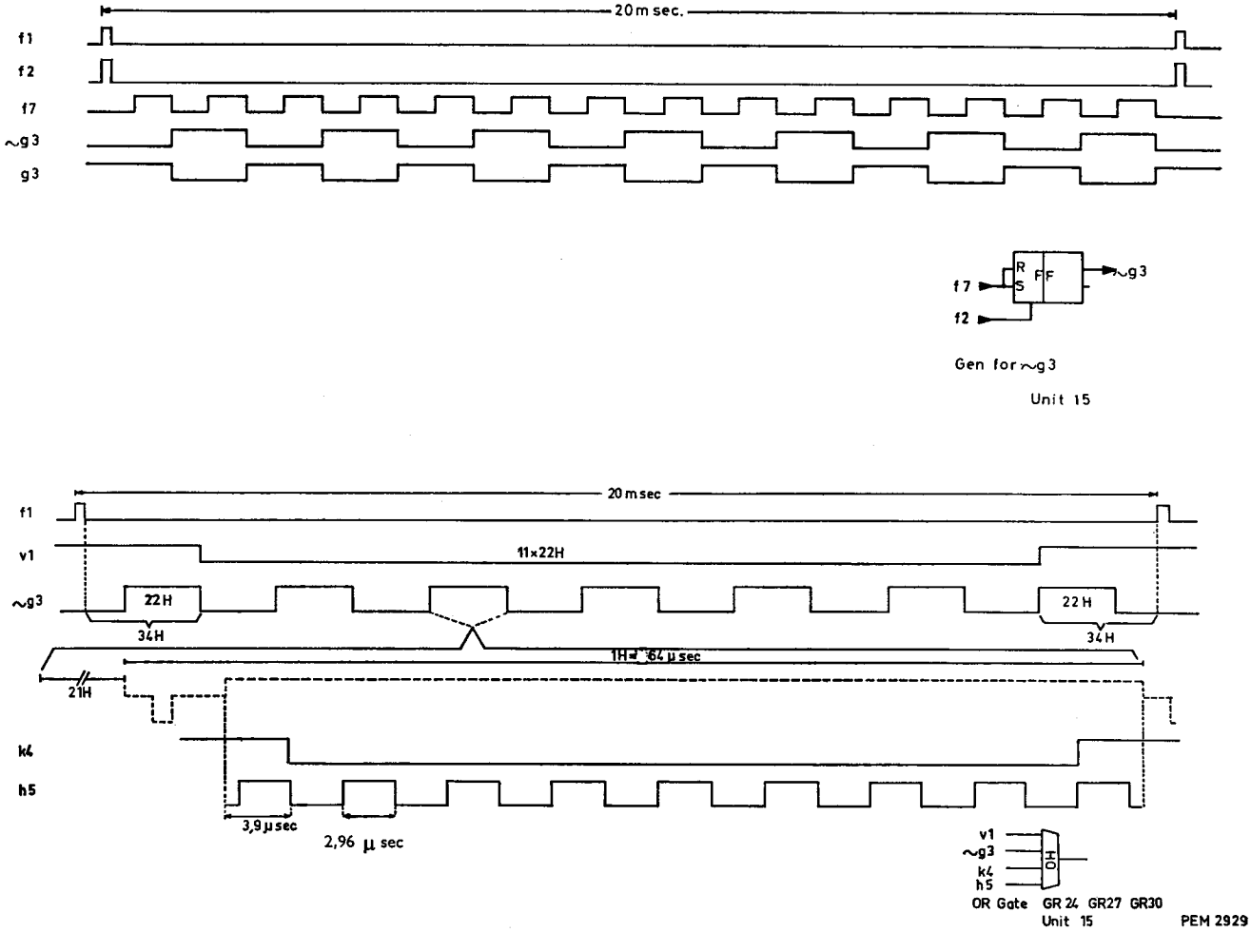


Fig. XXI-4 Pulse diagram for "~ g3"

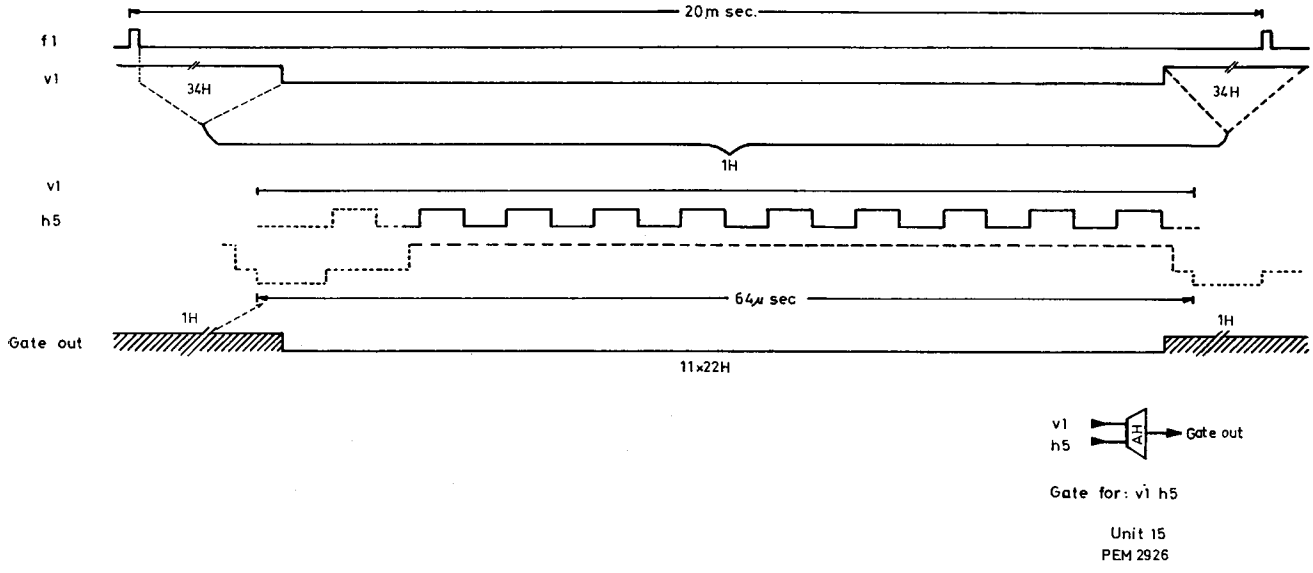


Fig. XXI-5 Pulse diagrams for "h5" and "v1"

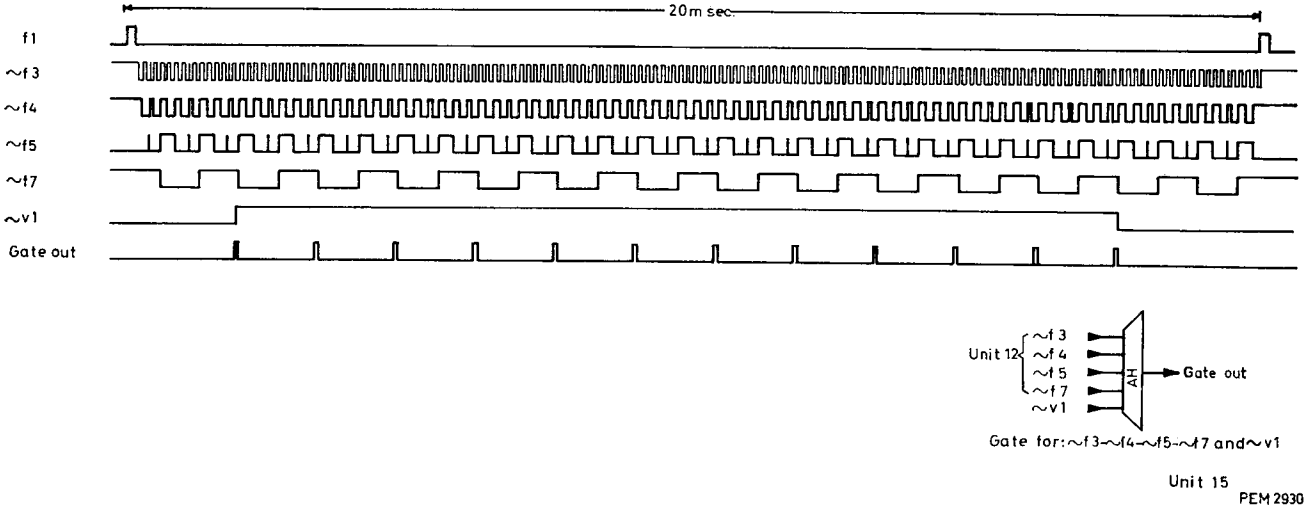


Fig. XXI-6 Pulse diagrams for "~ f3", "~ f4", "~ f5", "~ f7" and "~ v1"

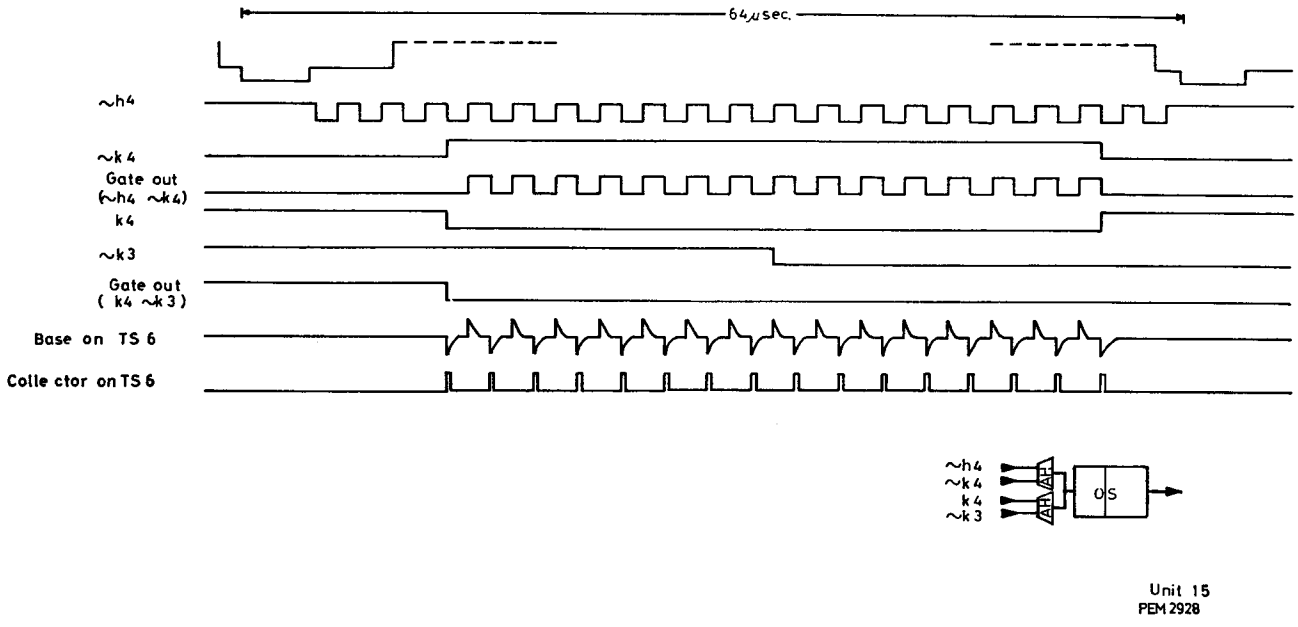


Fig. XXI-7 Pulse diagrams for "~ h4", "~ k3", „k4" and "~ k4"

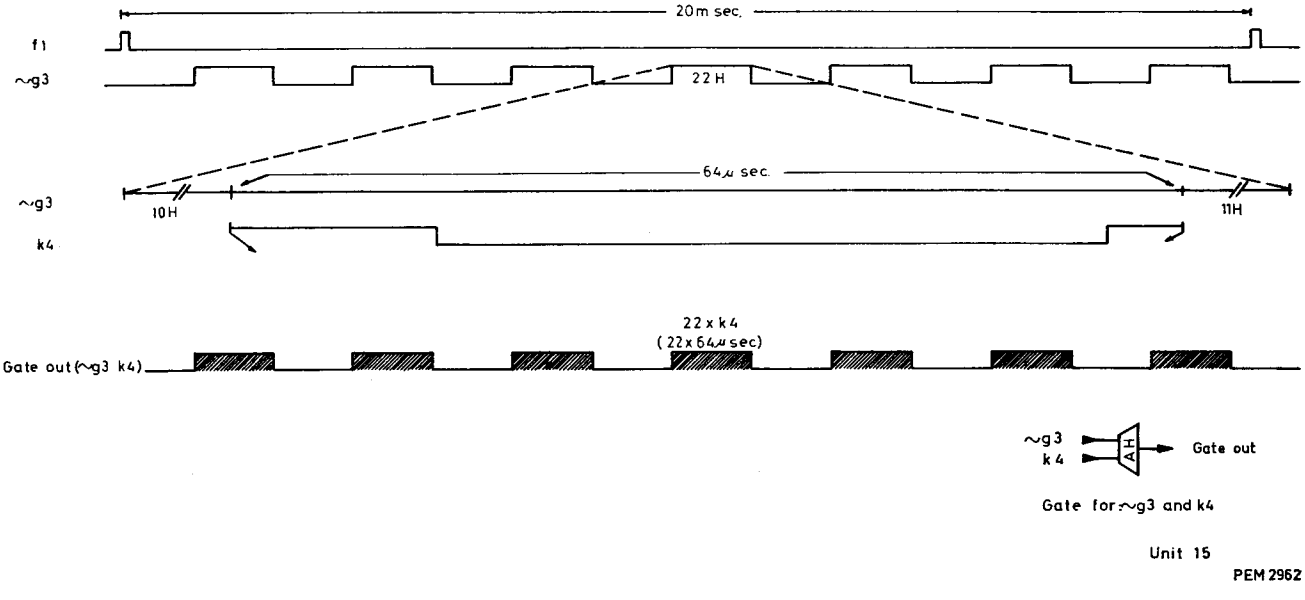


Fig. XXI-8 Pulse diagrams for "~ g3" and "k4"

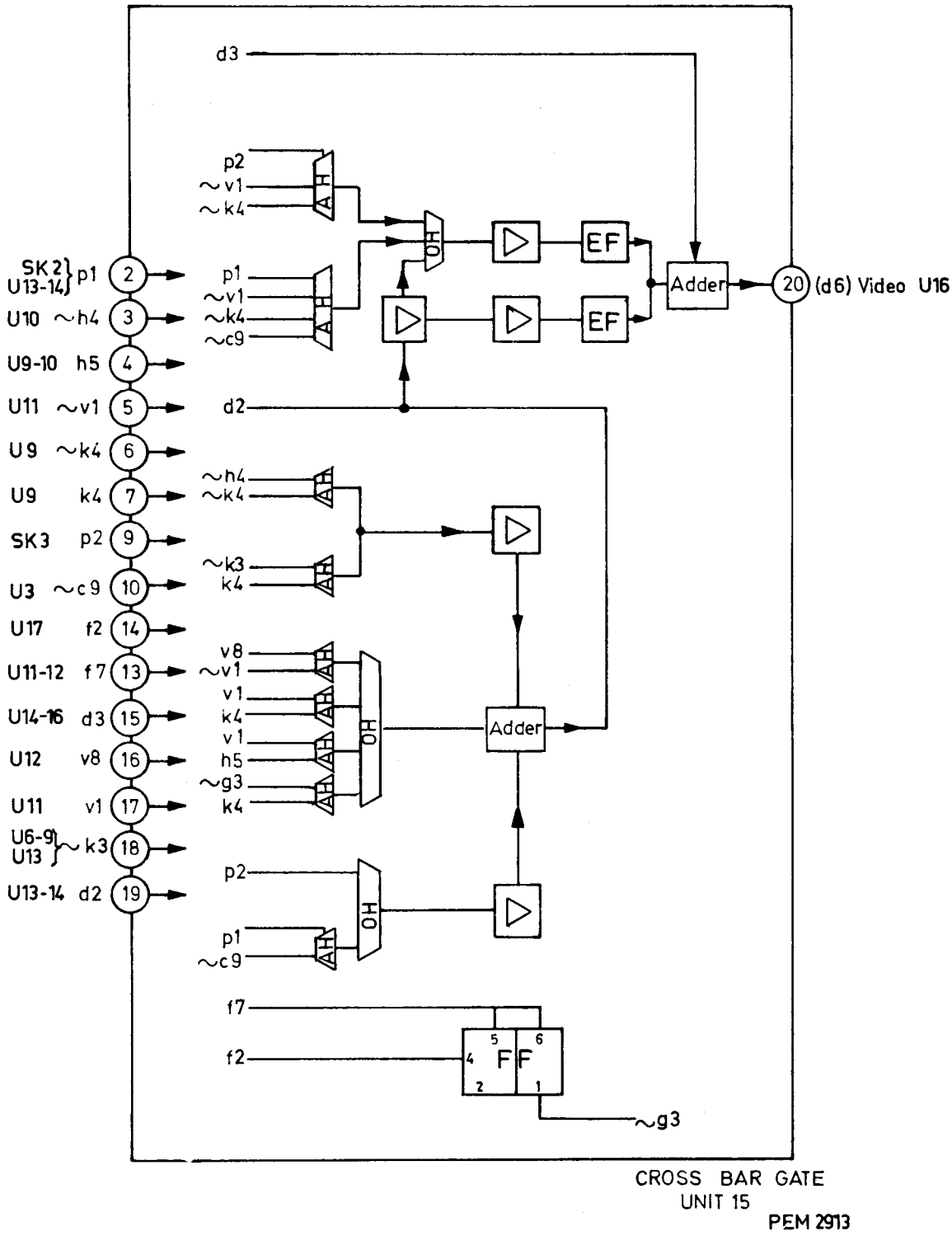


Fig. XXI-9 Block-diagram, Cross-bar gate, Unit 15

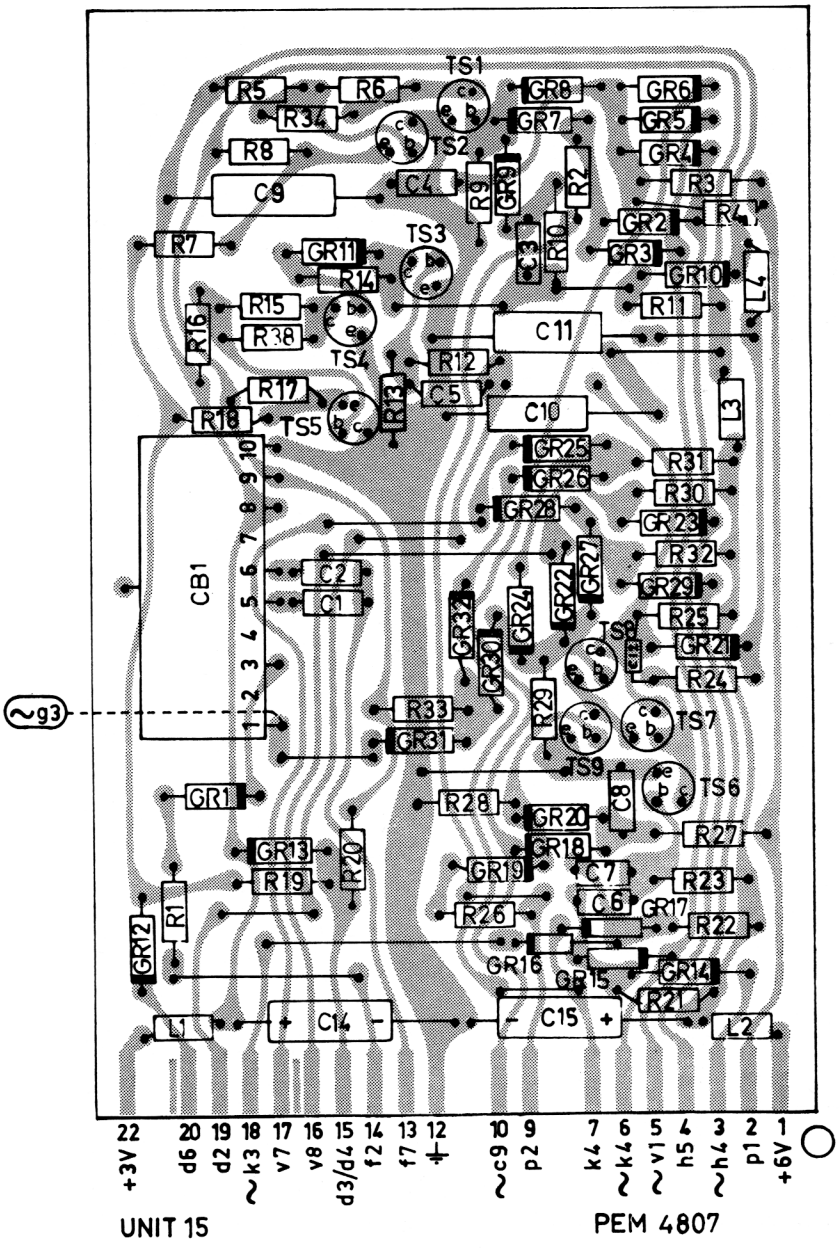
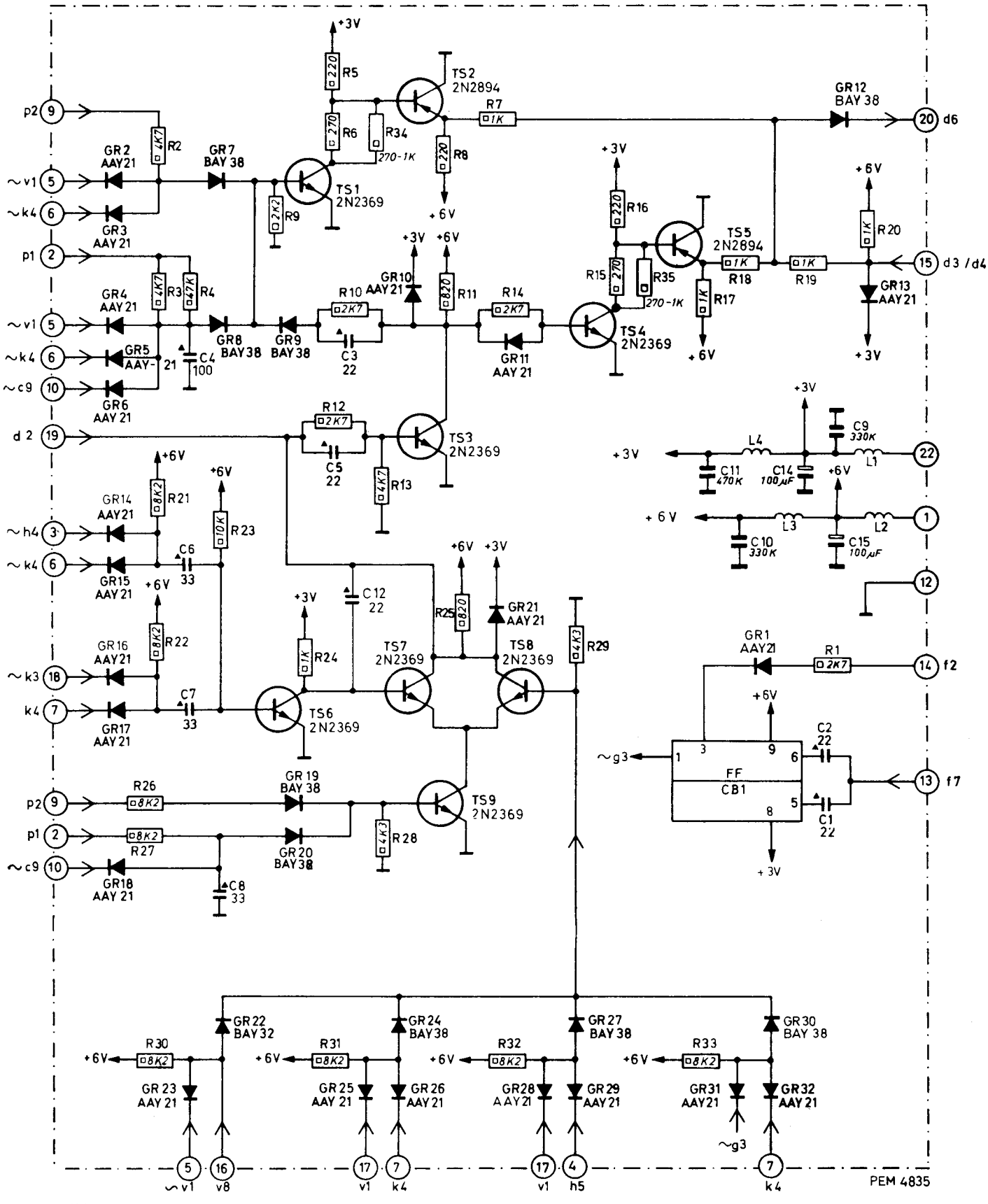


Fig. XX-10 Printed wiring board, Cross-bar gate, Unit 15



From version /06 the following is modified:
— GR 16 is of the type BA438 (4822 130 30256)
— C12 has become 68pF
— R8 has become 1k Ω

Fig. XXI-11 Circuit diagram, Cross-bar gate, Unit 15

XXII Unit 16

The output amplifiers

This unit contains two video output amplifiers, an extern-video input amplifier, a saw-tooth generator and a blank pattern generator.

Video amplifier II

In this circuit the video signal is combined with blanking and synchronizing pulses, and at the same time the black level is fixed.

The video-signal ("d6") is applied, via TS10, to amplifier TS11. TS12 together with TS11 also function as a black level clipper. The output current of TS11 is divided between TS12 and the resistors R39 and R40. The current through these resistors is constant and so adjusted by R40, that the emitter current in TS12 will be zero during the black level.

During the blanking pulse "a1", TS14 is in saturation and as a result, the signal to TS12 is short-circuited. This ensures a correct blanking of the signal, independent from the setting of the black livel clipper.

The synchronizing pulse "$\sim$ s1" is added, via TS13, to the complete video-signal and applied via the output amplifiers TS15 and TS16 to output II.

TS15-TS16 is a complementary feed-back amplifier having a high input and a low output impedance.

Video-amplifier I

In this circuit the black level clipper (TS4 . . . TS5), the blanking circuit (TS6) and the video-amplifier (TS8 . . . TS9) are identical to the amplifier described under video amplifier II.

However, it is possible to adjust the input sensitivity by means of R8.

It is also possible to add an external video information via amplifier TS1 . . . TS2.

The input impedance of the external video input is high, as a result of which the input impedance does not load the externally connected instruments (e.g. markers or text). The external video information, which is linearly added to the internal video and synchronizing pulses is applied, via TS8-TS9, to output I. The sync. amplitude is adjustable 0-200 % with potentiometer ("SYNC. AMPL.") at the front of the instrument so that the correct video-sync. ratio can be obtained.

The saw-tooth generator

This generator, consisting of TS18-TS19, is controlled by the line blanking pulse "a1".

When push-button SK6 (front) is not depressed, TS17 and TS18 are continuously into saturation due to the supplied level "P5" (+6 volt). If SK6 is depressed the +6 V level disappears (indicated with "$\sim$ p5") and TS17 and TS18 are driven into saturation by the blanking pulse "a1".

However, between blanking pulses, TS17 and TS18 are cut-off and C10 is charged via TS19. During the time TS18 is saturated (blanking), C10 is discharged via this transistor. The resulting saw-tooth (d4) is applied, via emitter-follower TS20, to the cross-bar gate (unit 15). The saw-tooth is linear because diode GR3 keeps the base voltage of TS19 and also the charge-current to C10 constant.

Blank pattern generator

When push-button SK8 ("BLANK PATTERN") is depressed, TS21 produces a voltage across R20 (unit 15) representing the blank pattern. The grey value of this pattern is dependent on the current through TS21. This current is adjustable with the potentiometer at the front of the instrument, marked "GREY VALUE".

Checking and adjusting

Measuring equipment:
Oscilloscope: e.g. PHILIPS PM 3330.
Depress SK1 "COMPL. PATTERN".

Amplitude and set-up "OUTPUT II"

Connect the oscilloscope to BU2 "OUTPUT II".
Terminate "OUTPUT II" with 75 Ω.

The video signal is adjusted without set-up (R40) while the amplitude between white- and black level is adjusted to 700 mV ± 50 mV by R58 so that the complete video signal is 1 $V_{p\text{-}p}$. However, set-up can be introduced by readjusting R40 and, if necessary, by selecting another value for R58 (820 Ω . . . 5.6 kΩ).

Amplitude and set-up "OUTPUT I"

Connect the oscilloscope to BU1 "OUTPUT I".

Terminate "OUTPUT I" with 75 Ω.

The video signal is adjusted without set-up (R25) while the amplitude between white- and black level is adjusted to 700 mV ± 50 mV by R8 so that the complete video signal is 1 V_{p-p}. However, set-up can be introduced by readjusting R25. In that case it is necessary to readjust R8.

R8 can also be used for adjusting the amplitude of the video signal between white- and black level from 0.5 V_{p-p} to 1 V_{p-p}.

Amplitude of the sync. signal "OUTPUT I"

The complete video signal should be 1 V_{p-p}.

The sync. signal should be 300 mV ± 50 mV.

If not, readjust R2 ("SYNC. AMP." front of the instrument).

Amplitude of the saw tooth

Depress SK6 "SAW TOOTH".

The amplitude between white- and black level should be 700 mV ± 50 mV.

If not, select another value for R56 (2.2 kΩ . . . 10 kΩ).

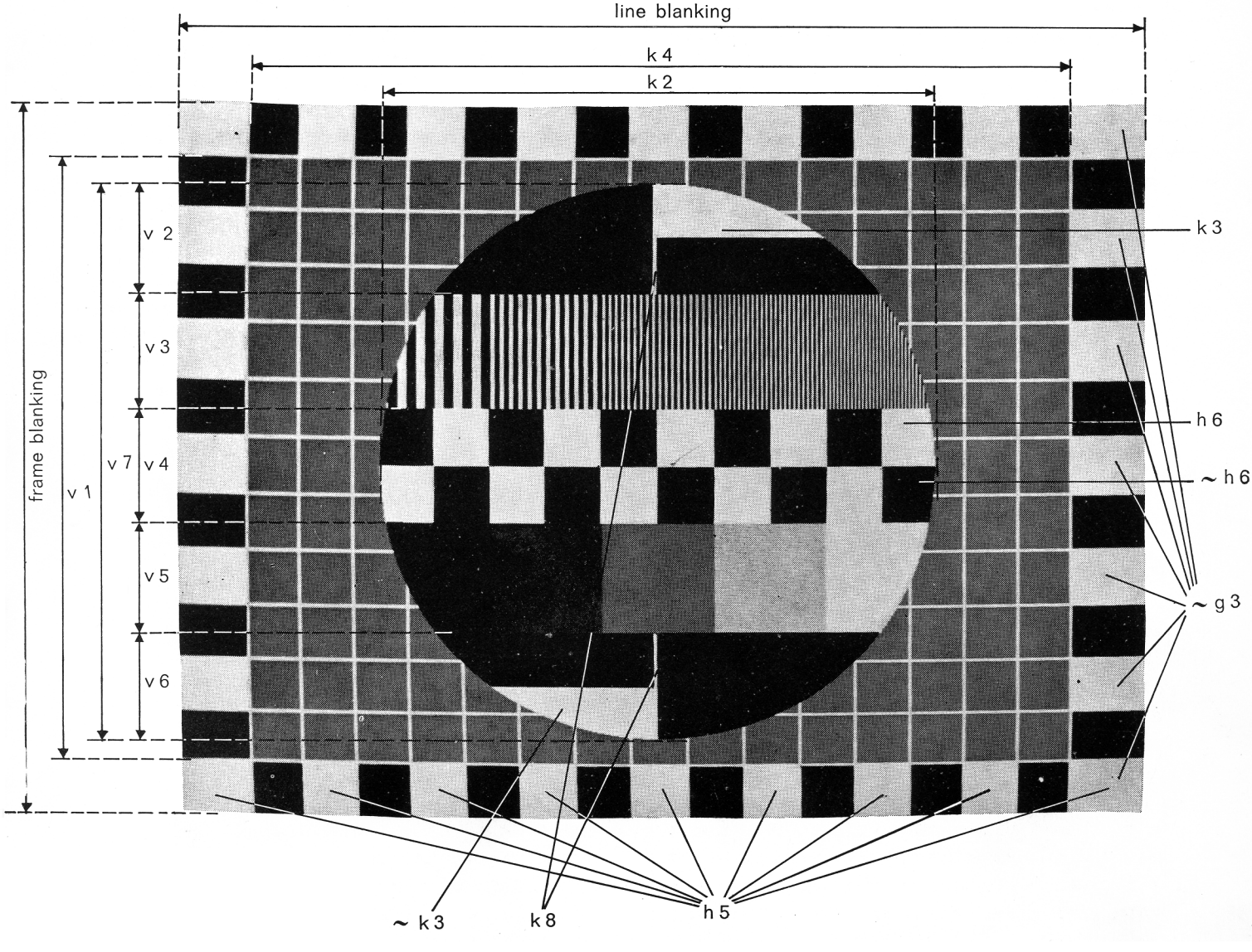


Fig. XXII-1 Test pattern

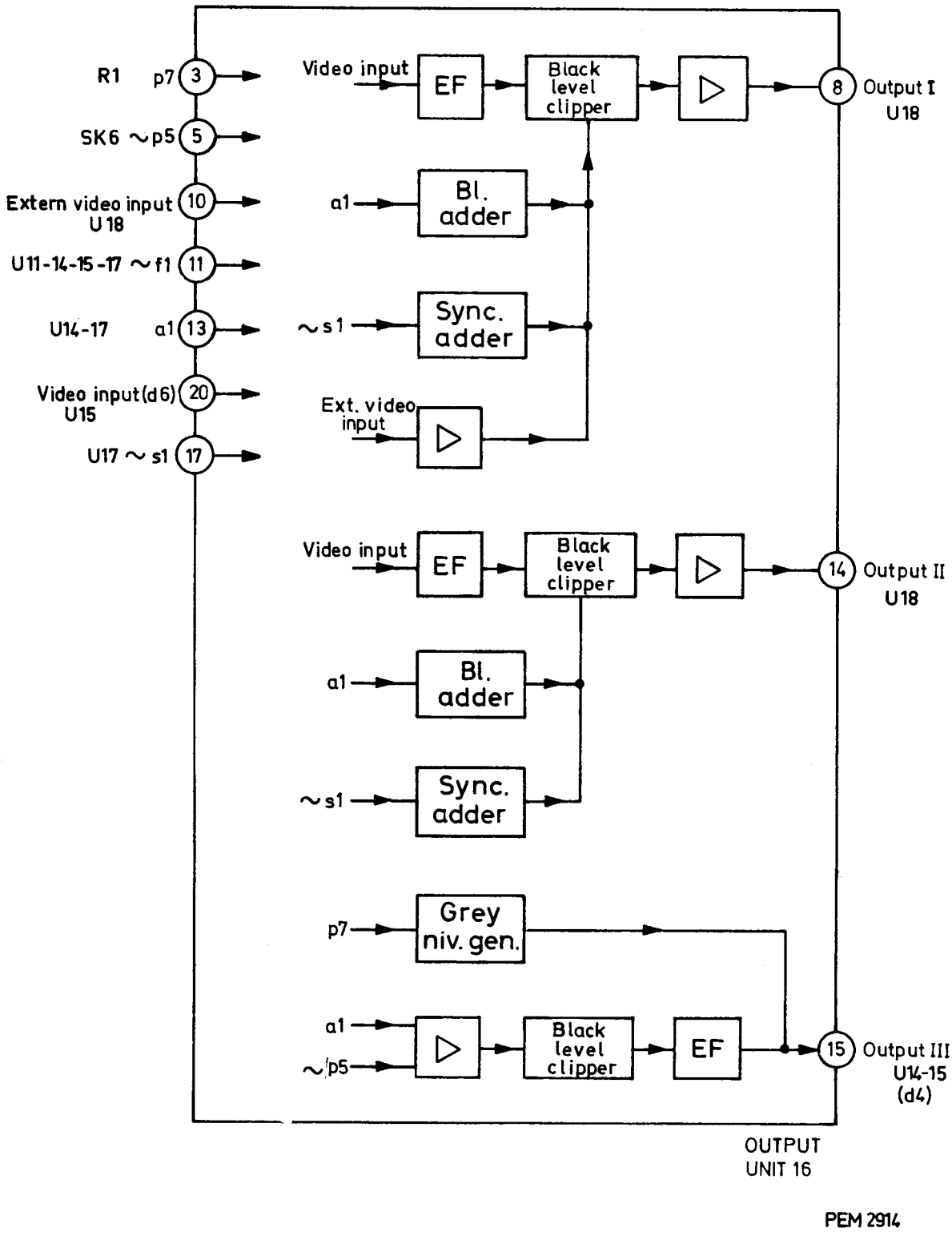


Fig. XXII-2 Block-diagram, video output, Unit 16

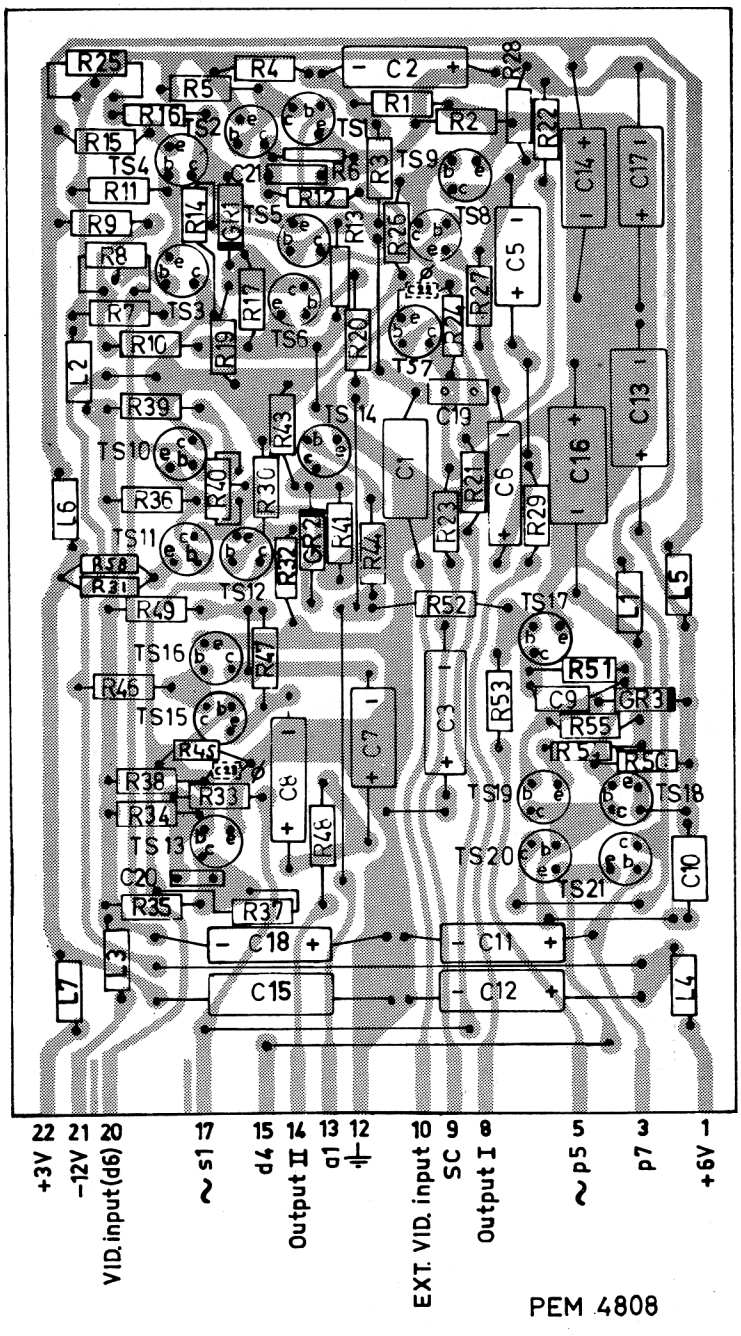


Fig. XXII-3 Printed wiring board, video output, Unit 16

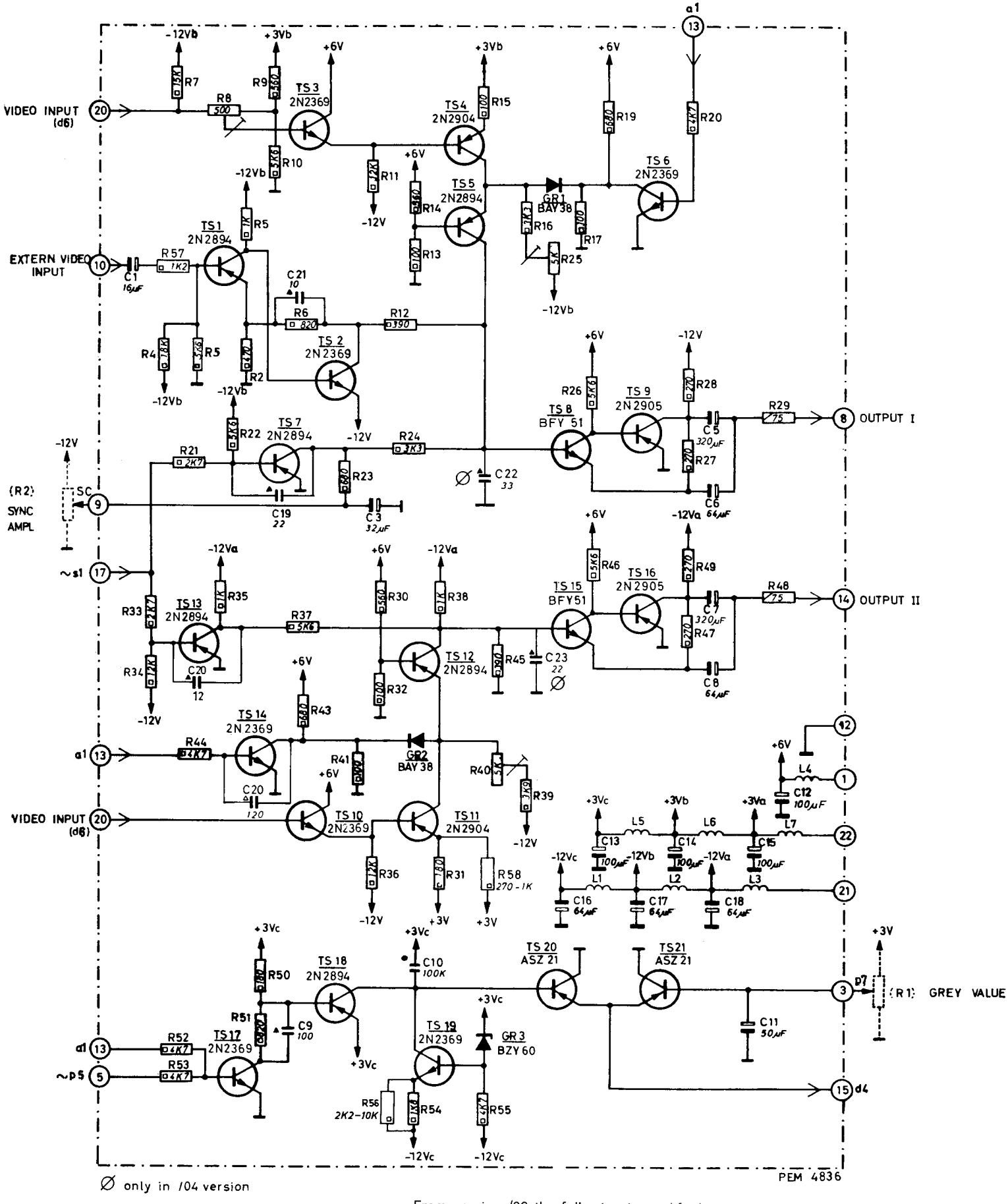


Fig. XXII-4 Circuit diagram, video output, Unit 16

From version /06 the following is modified:
- R7 has become 13kΩ
- R31 has become 150Ω
- R50 has become 1k Ω
- R58 has become 1k Ω - 5k Ω selected.

XXIII Unit 17

The input amplifier

This circuit comprises input amplifiers for the blanking signal ("a1"), the composite sync. signal ("∿ s1") and the generators for the "f", "g" and "h" pulses.
The pulses generated (e.g. PHILIPS PM 5530) are accurately specified as regards amplitude and pulse shape, but could be distorted by the cable distribution network due to reflections, wrong termination, cable losses, hum etc.
Fig. XXIII-1 and 2 show some examples of typical distortion. This distortion must be eliminated to ensure proper operation. Therefore all input circuits are provided with special circuits for eliminating the distortion.

Input amplifier for the blanking signal
The blanking signal is applied to TS1-TS2 via terminal 21. Diodes GR1 and GR2 limit the input signal symmetrical with respect to zero level at 12 $V_{p\text{-}p}$.
The bias of TS1 is selected so that only the centre part of the pulse is amplified (see Fig. XXIII-3). This pulse appears with correct shape across the emitter resistor R3. The keyed clamping circuit TS3 serves to eliminate hum from the signal. This circuit operates in the on-off mode due to the sync. pulses applied to the base of TS4.

At each sync. pulse the base voltage of TS4 is automatically clamped, via R6 and C3, to half the pulse voltage level, so that possible hum in the signal is eliminated.
The blanking pulse "a1" is applied to unit 14 where it is used to start and stop the generator for the definition lines, and to unit 16 to provide the required blanking for the video signal.

Input amplifier for the sync. pulses
The sync. pulses from terminal 20 are applied to amplifier TS5 . . . TS8 which is identical to the amplifier of the blanking input.
The distorded part of the pulse and possible hum will be eliminated in this circuit.
The output signal "∿ s1" is applied, via TS10, to the frame and line generators and via TS9 and terminal 17 to unit 16 where it is used to provide the required sync. for the video signal.

Generator for the "∿ f1" and "f2" pulses
The frame pulses "∿ f1" and "f2" are formed in the one-shot multivibrator TS11-TS12 (see Fig. XXIII-4). The length of the generated pulses is determined by R27 and C14.
To ensure correct triggering of the multivibrator it is controlled by negative going pulses which are derived from the first pre-equalizing pulse.
The sync. signal coming from TS10 is first differentiated by C11 and R24 to obtain this trigger pulse. As shown in Fig. XXIII-5 the R-C time is selected so that the equalized pulses retain their back porch (GR9 eliminates the positive-going spikes).
After being differentiated again by C12 and R25 the pulses as shown in Fig. XXIII-6 arise.
The negative going pulses are used to trigger the multivibrator. The R-C time of this multivibrator is selected so that the trailing edge (back porch) of the "f1" pulse starts at the first line of the first field and at the second line of the second field, after the post-equalizing pulses. The "∿ f1" pulse is used to set the pulse generator in unit 11. The output pulse "f1" from TS11 is applied to the one-shot generator TS14 which operates only during the trailing edge of this pulse. The width of the output pulse "f2" of TS14 is determined by C18 and R37.
The "f2" pulse is used in unit 12 to trigger the vertical divider.

Generator for the "g5" and "∿ g5" pulses
This generator, formed by CB1 and AND-gate GR13-GR14, is controlled by the "∿"1"" and "h1" pulses.
The one-shot TS13 supplies the control pulses for CB1 which are derived from the "∿ f1"" pulses.
The "g5" and "∿ g5" pulses are used to control the interval decoder in unit 8.

Generator for the "g4" and "∿ g4" pulses
This generator, consisting of CB2 and AND-gate GR15-GR16, is set to zero by the "∿ f1" pulse and is controlled by the "g2" and "v4" pulses.

The "g4" and "∿ g4" pulses are used to control the line-selector register in unit 7.

Generator for the "h1" and "∿ h1" line pulses
The line pulses are generated in the one-shot multivibrator TS17-TS18. The duration of these pulses are controlled by C24 and R49-R50. The correct width (4.0 μs) is obtained by means of potentiometer R50. The line generator is not triggered directly by the composite sync. signal but via the one-shot multivibrator TS15-TS16 to prevent the generator from being triggered at twice the line frequency during the equalizing pulses.
As the discharge time of this multivibrator is more than half a line time (>32 μs), it is only triggered by the active equalizing pulses.

The "h1" pulse is applied to unit 9 to trigger the generator for the "k5" pulses. These pulses are used to control the forward or down-counting of the circle register.
The "∿ h1" pulses are applied to the units 3, 4, 9, 10 and 12 to trigger the various generators in these units.

Checking and adjusting
Measuring equipment:
Oscilloscope: e.g. PHILIPS PM 3330.

Width of "h1" pulse
Connect the oscilloscope to terminal 4.
The width of the "h1" pulse should be 4.0 μs ± 0,1 μs.
If not, readjust R50.

Situation of the "f2" pulse
The "f2" pulse should be placed as shown in oscillogram "f2" of Fig. XXIII-7.
If not, readjust R27.

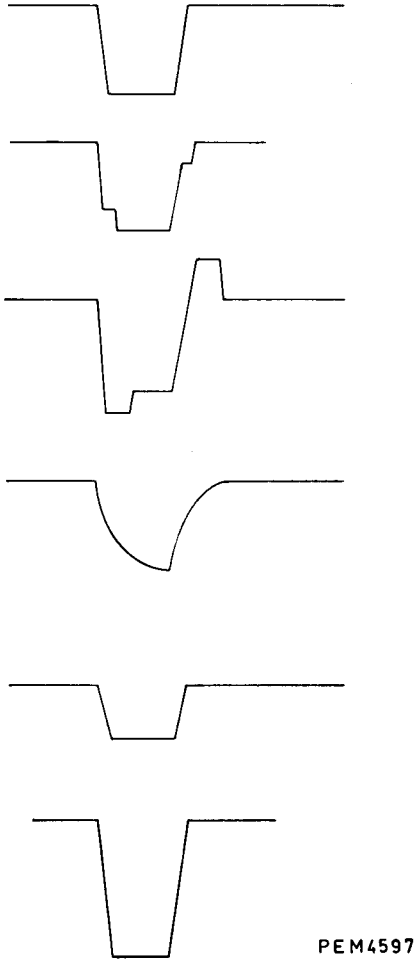


Fig. XXIII-1 Pulse diagram of typical distortions

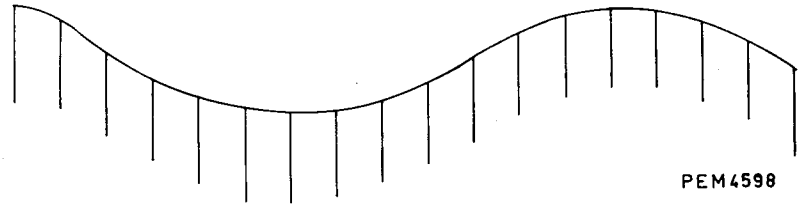


Fig. XXIII-2 Pulse diagram of typical distortion

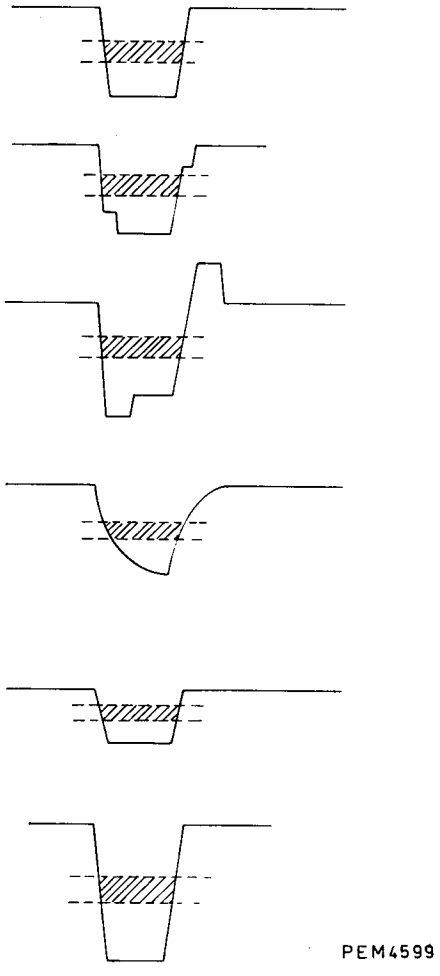


Fig. XXIII-3 Pulse diagram

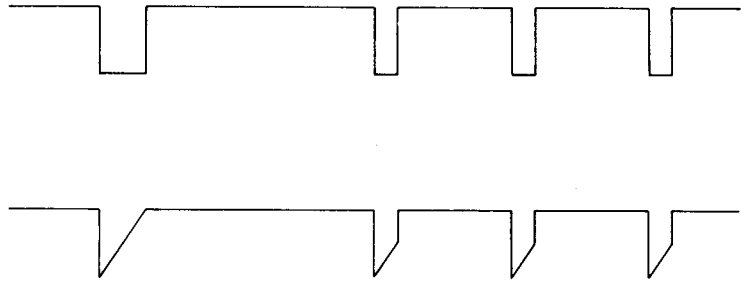


Fig. XXIII-5 Pulse diagram

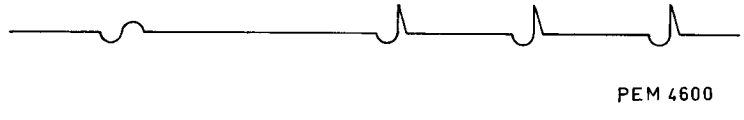


Fig. XXIII-6 Pulse diagram

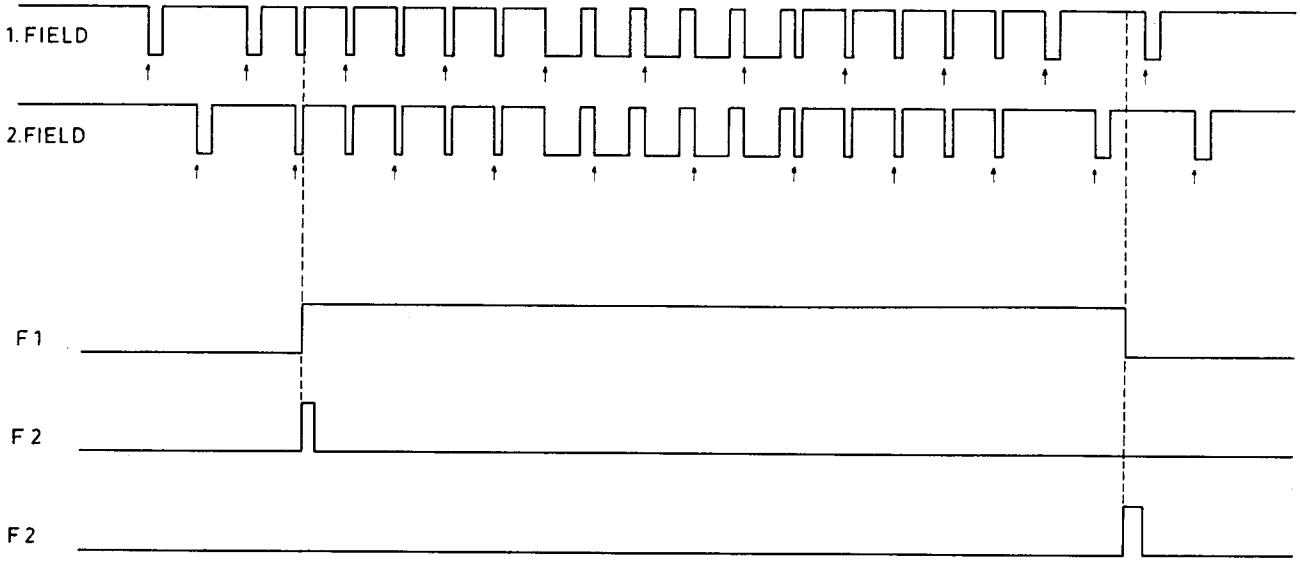
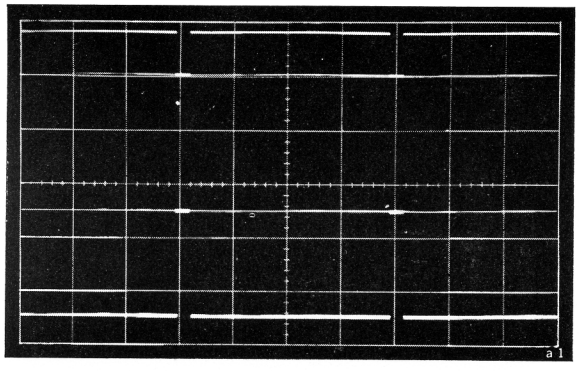
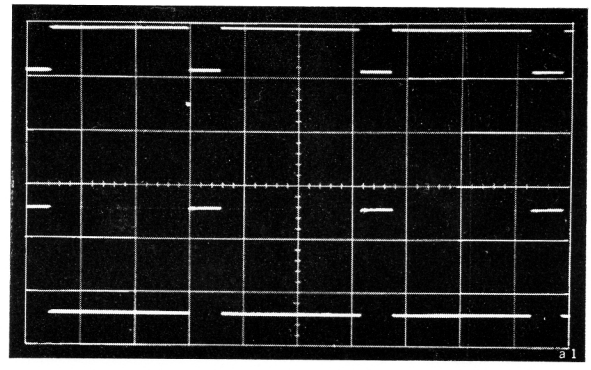


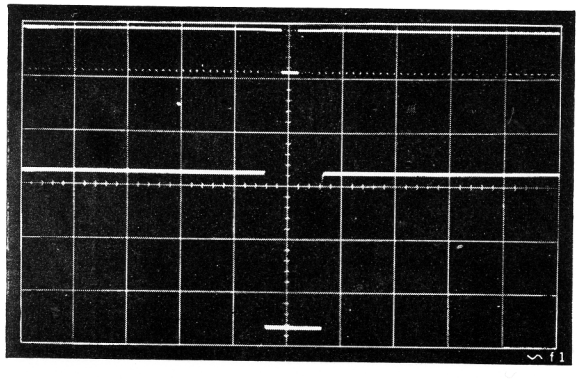
Fig. XXIII-4 Pulse diagrams for "f1" and "f2"



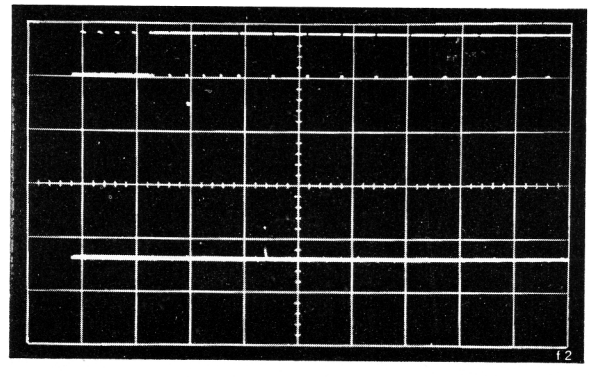
a1
2 V/cm 5 ms/cm
reference: blanking



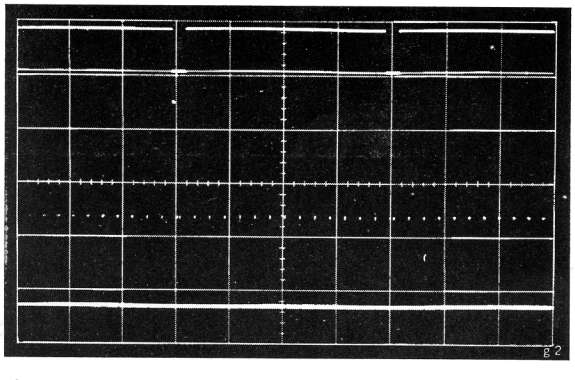
a1
2 V/cm 20 μs/cm
reference: blanking



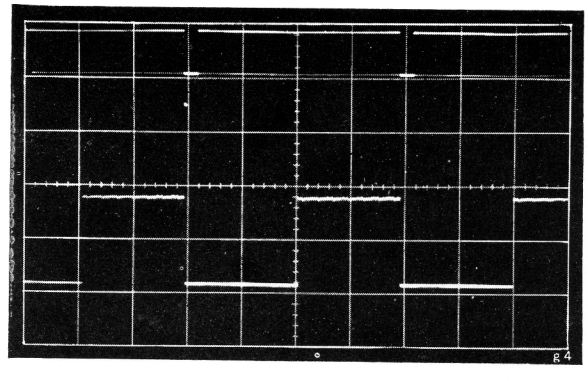
~ f1
2 V/cm 0.5 ms/cm
reference: sync.



f2
5 V/cm 0.1 ms/cm
reference: sync.

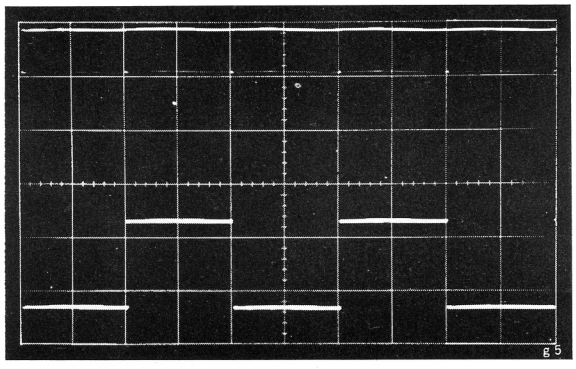


g2
2 V/cm 5 ms/cm
reference: blanking

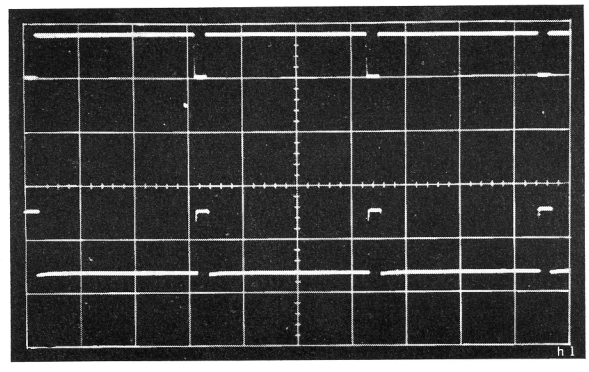


g4
2 V/cm 5 ms/cm
reference: blanking

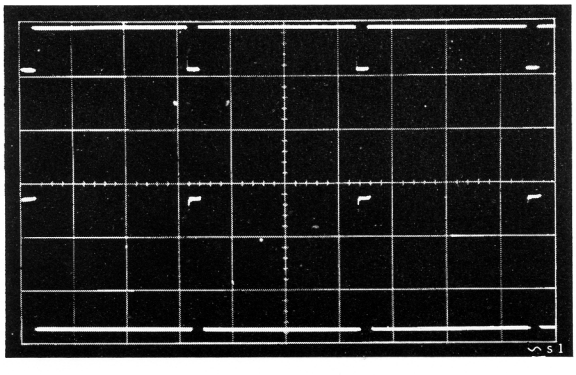
Fig. XXIII-7 Oscillograms, Unit 17



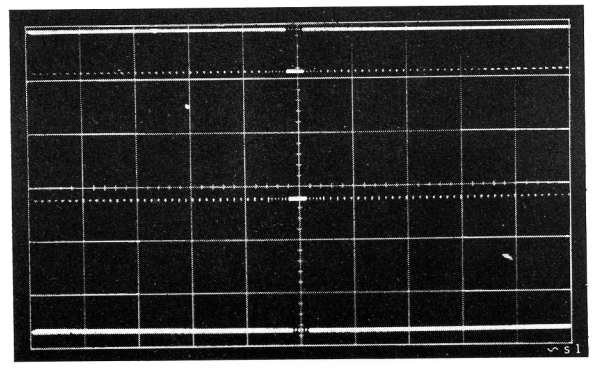
g5
2 V/cm 10 ms/cm
reference: sync.



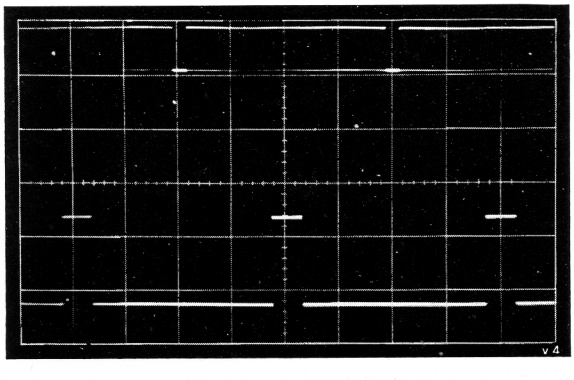
h1
2 V/cm 20 μs/cm
reference: sync.



~ s1
2 V/cm 0.5 ms/cm
reference: sync.



~ s1
2 V/cm 20 μs/cm
reference: sync.



v4
2 V/cm 5 ms/cm
reference: blanking

Fig. XXIII-7 Oscillograms, Unit 17

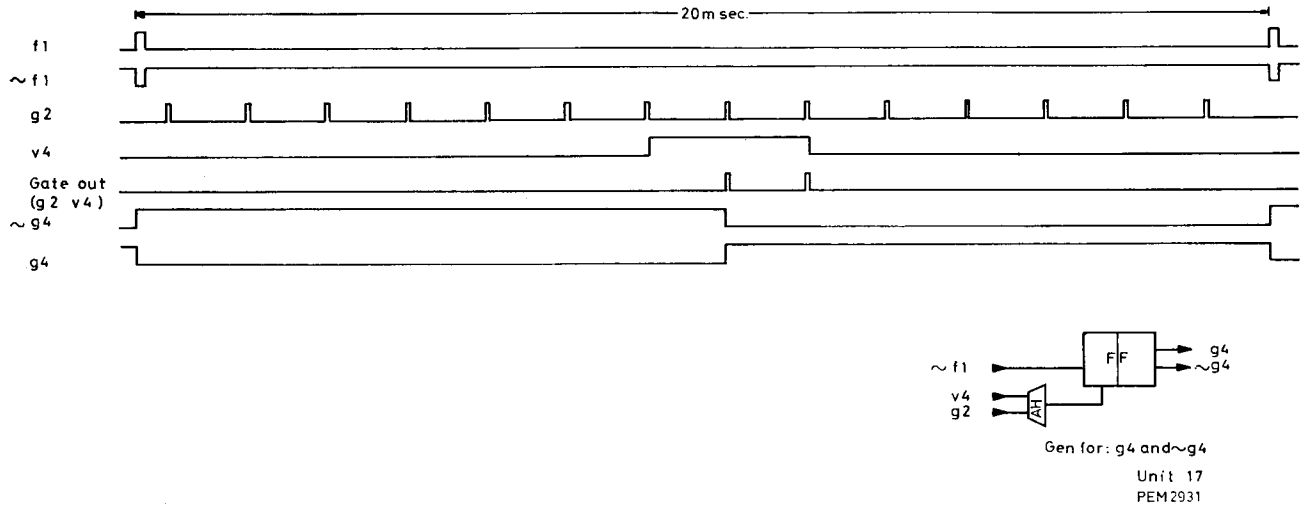


Fig. XXIII-8 Pulse diagrams for "g4" and "$\sim$ g4"

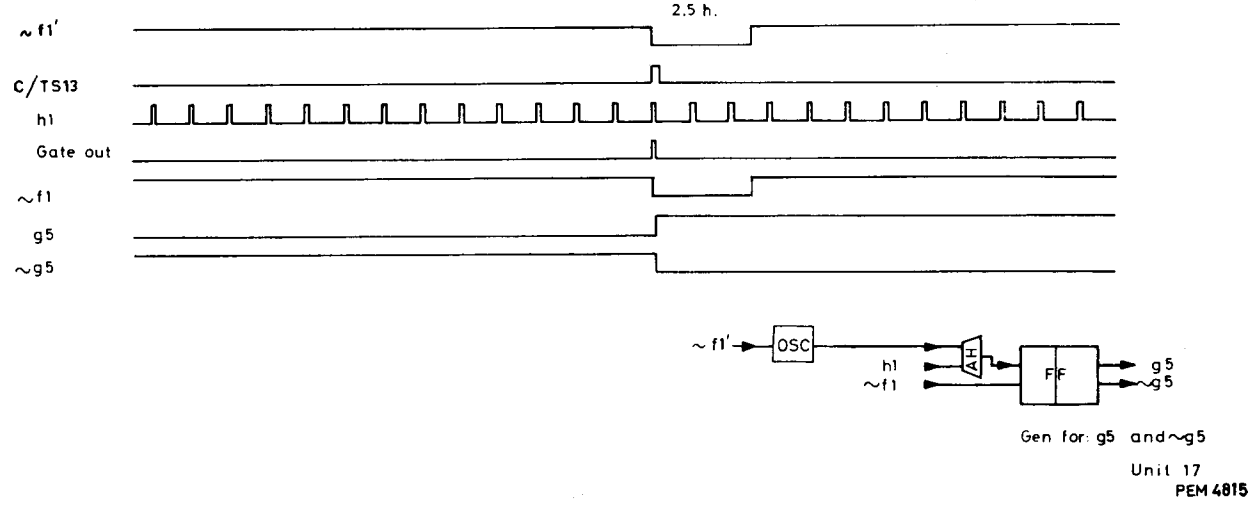


Fig. XXIII-9 Pulse diagrams for "g5" and "$\sim$ g5"

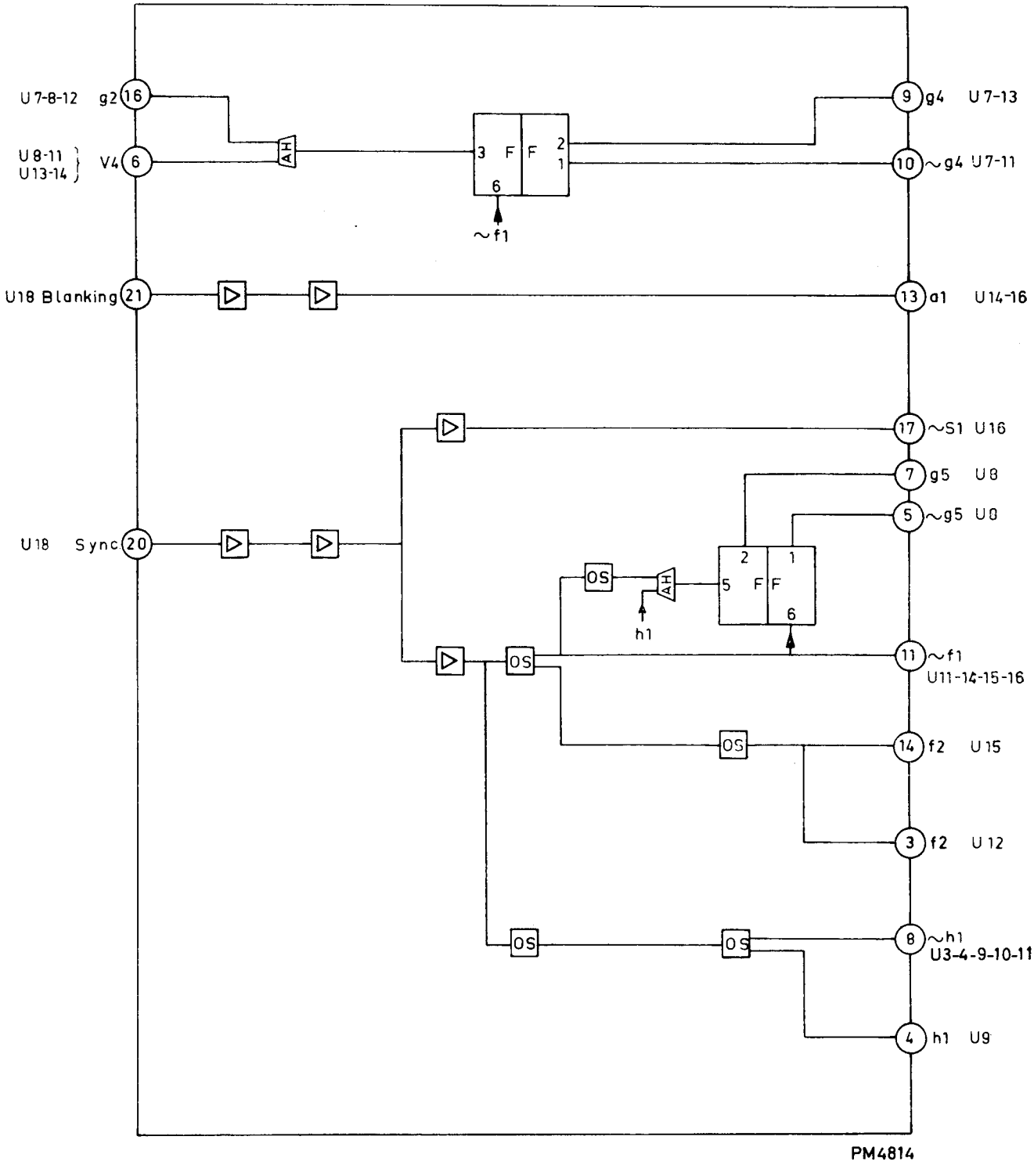


Fig. XXIII 10 Block-diagram, input amplifier, Unit 17

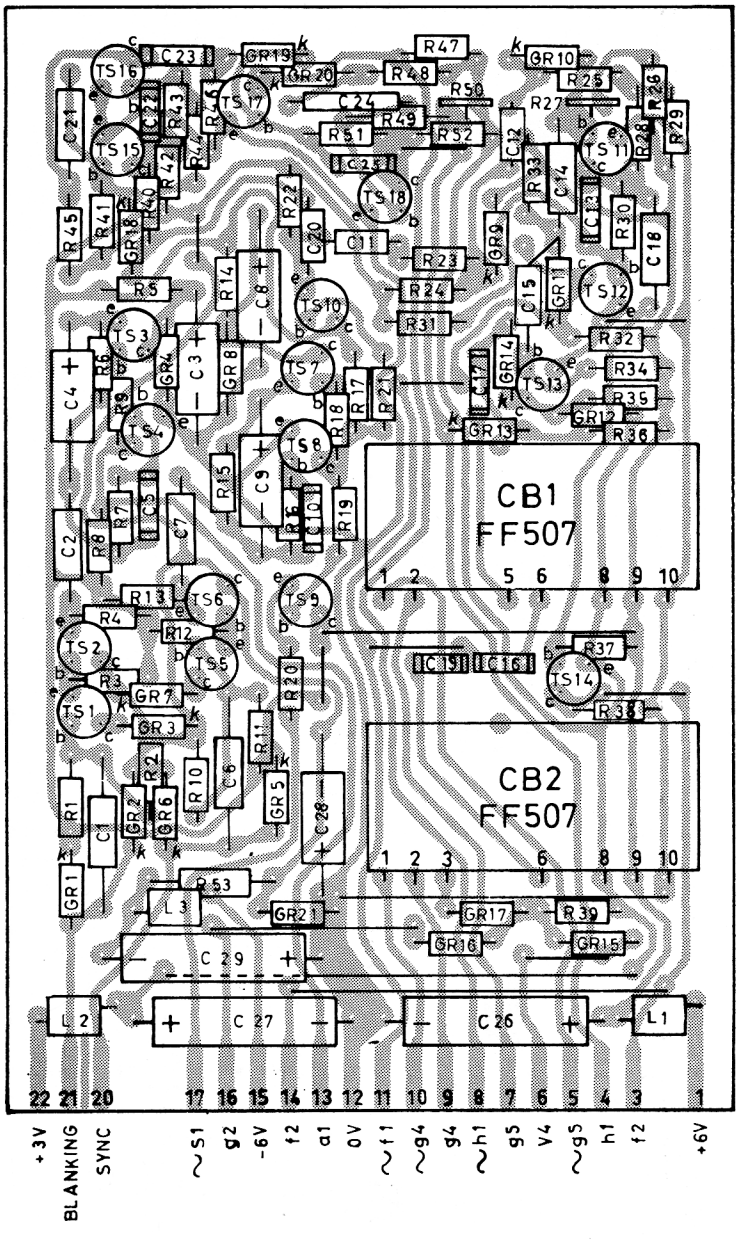
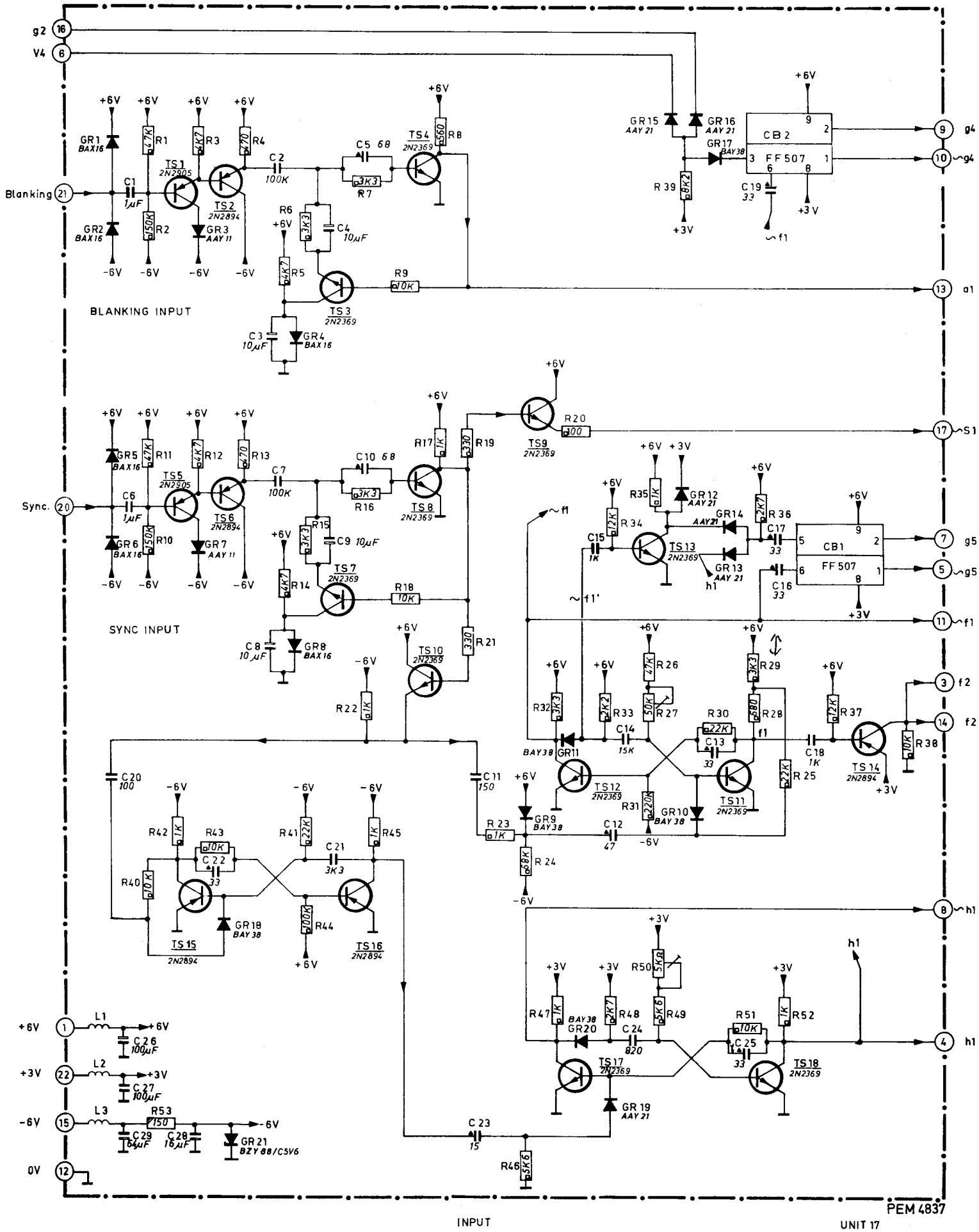


Fig. XXIII-11 Printed wiring board, input amplifier, Unit 17

Fig. XXIII-12 Circuit diagram, input amplifier, Unit 17


g2
V4
Blanking
Sync.
BLANKING INPUT
SYNC INPUT
CB2
CB1
FF 507
TS1 2N2905
TS2 2N2894
TS3 2N2369
TS4 2N2369
TS5 2N2905
TS6 2N2894
TS7 2N2369
TS8 2N2369
TS9 2N2369
TS10 2N2369
TS11 2N2369
TS12 2N2369
TS13 2N2369
TS14 2N2894
TS15 2N2894
TS16 2N2894
TS17 2N2369
TS18 2N2369
GR1 BAX16
GR2 BAX16
GR3 AAY11
GR4 BAX16
GR5 BAX16
GR6 BAX16
GR7 AAY11
GR8 BAX16
GR9 BAY38
GR10 BAY38
GR11 BAY38
GR12 AAY21
GR13 AAY21
GR14 AAY21
GR15 AAY21
GR16 AAY21
GR17 BAY38
GR18 BAY38
GR19 AAY21
GR20 BAY38
GR21 BZY88/C5V6
+6V
-6V
+3V
0V
f1
f1'
h1
g4
g5
a1
S1
f2
L1
L2
L3
INPUT
PEM 4837
UNIT 17

XXIV Unit 18

The connection board

The mounting plate for connectors BU3 . . . BU10 is secured to a printed wiring board. This assembly is unit 18 (detachable).

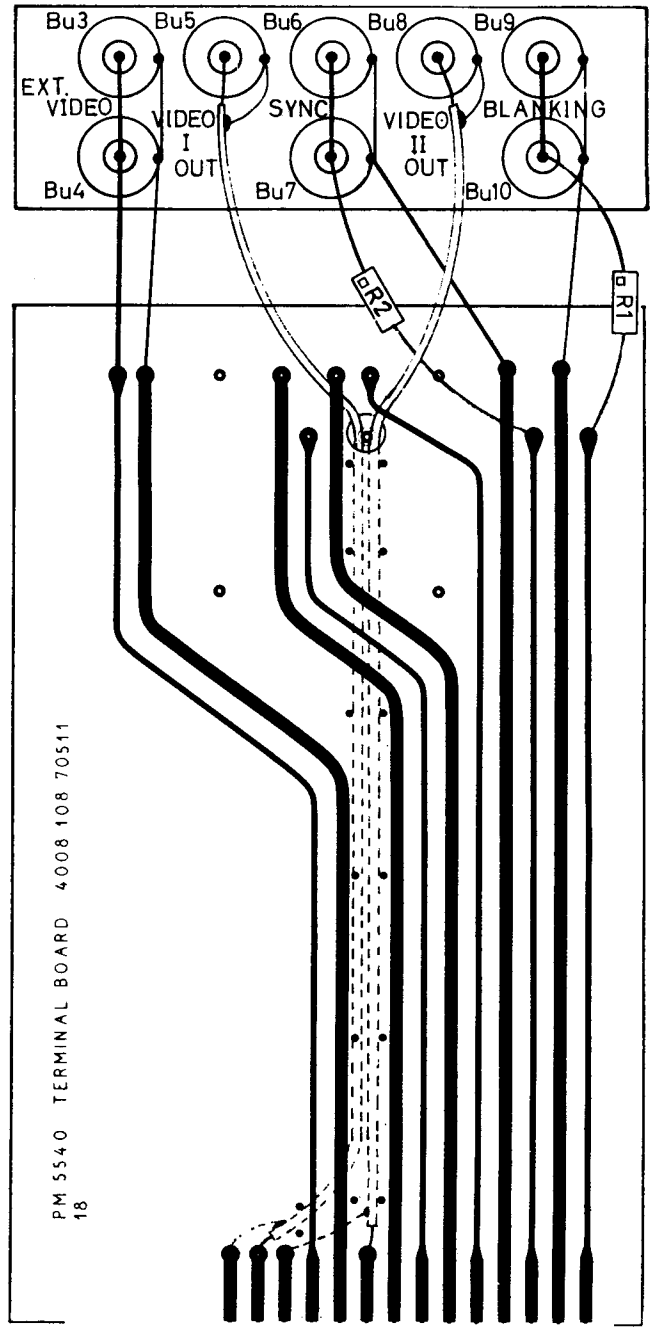


Fig. XXIV-1 Printed wiring board, connection board

PEM4810

XXV Description of basic circuits

I. Definitions

In the professional pattern generator PM 5540 most circuits are built up by means of logic circuits (AND and OR-gates) as wel as high speed flip-flop circuit blocks FF 507.

In this description the following terms are used:

"0" corresponding to approx. 0 V = low (L)
"1" corresponding to approx. +6 V = high (H)
For a pulse 180° phase-inverted, the sign $\sim$ is used for the pulse denomination. It means that
$\sim$ "0" = "1" or
$\sim$ "1" = "0"
Often the sign $\sim$ is called "not" or "false".
A rectangular pulse is produced when the signal level for a moment is changed from "0" to "1", and then again assumes the value of '0". If such a rectangular pulse is differentiated, first a positive RC-pulse will appear, and then a negative one, as shown in Fig. 1.

II. Gates and flip-flops

A. AND and OR-gates – level controlled pulse gates

When the content of a binary counter or a binary register is to be decoded, AND or OR units are used.
Fig. 2 shows and AND-gate for high (AH) With "1" on the terminals W1, W3 and W5, Q1 will be "1"while Q1 will be "0" if only of the terminals is "0". The OR-gate for high (OH) is shown in Fig. 3, from which it

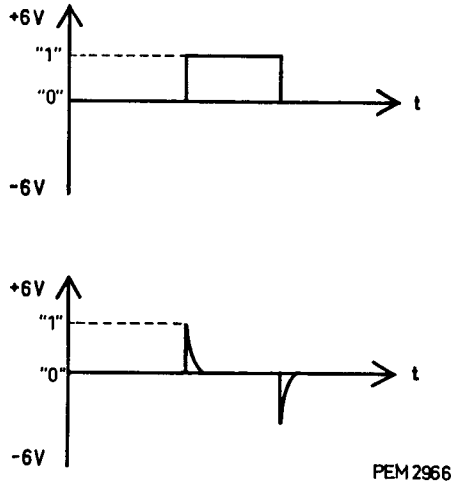


Fig. 1

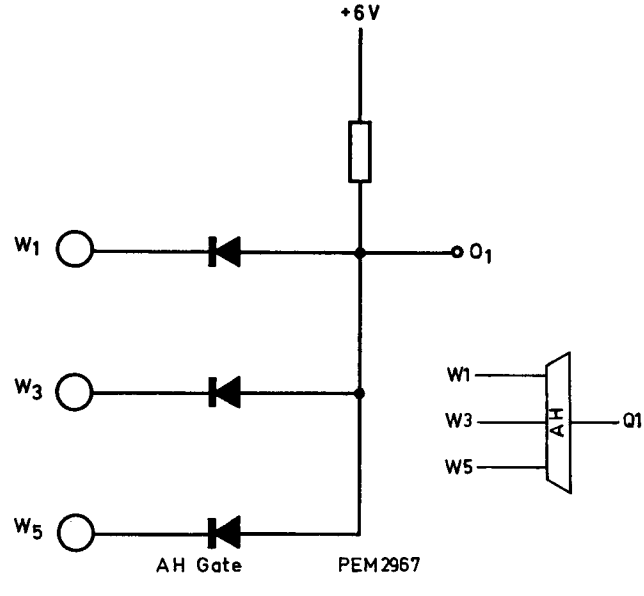


Fig. 2

may be seen that Q1 will be "1" if only the level of one of the terminals W1, W3, W5 is "1".
If a pulse is to be blocked or passed, controlled by a d.c. signal, a level controlled pulse gate is used, as shown in Fig. 4. In Fig. 4a the function is indicated if a PNP-transistor is connected to the output of the pulse gate. It is shown that a negative pulse appears at the base if the signal level at G is "0", while no pulse will appear when the signal level is "1".

B. The flip-flop

The flip-flop FF507 (Fig. 5a) is a bistable high speed multivibrator.
By interconnecting the two a.c. inputs R and S a binary counter is made, as the built-in pulse gates controlled by the collectors always direct a negative pulse to the conducting transistor, which is blocked in this way, by which the flip-flop changes to its other stable position.

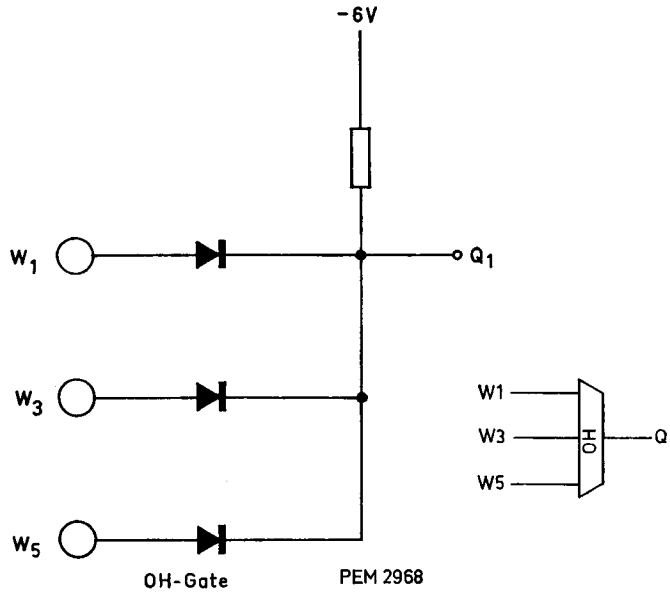


Fig. 3

III. Counters

A. Cascade connection of binary counters

A binary counter unit can be constructed by means of an FF(Fig. 6). If a rectangular pulse is applied to one of the terminals R or S, a differentiation takes place, by which the negative RC pulse appears at the base of the conducting PNP transistor, so that the latter is cut off, and the collector voltage jumps from "0" to "1". If the terminals R and S are interconnected, the transistors are cut off alternately as the collector voltages via the pulse gate will automatically direct the negative pulse to the base of the conducting transistor. In fig. 7 it is shown how the signal levels vary if a rectangular pulse is applied to the interconnected inputs. It may be seen that the frequency of the output signal is half the frequency of the input signal, so that a dividing by 2 has taken place.

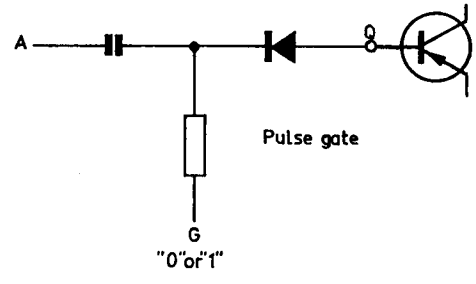


Fig. 4

If the signal at Q is applied to another FF, another dividing by two of the frequency will be effected. Any desired number of units can be cascade connected, and thus a counter can be composed which for n stages will halve the frequency n times, and which contains 2n different combinations of the positions of the flip-flop. Below a counter consisting of 4 stages (8:1 divider; see fig. 8) will be explained. If it is assumed that all flip-flops are in the position that all left-hand transistors are cut off ($\sim$ Q, Q = "1", "0"), the table shows the states of all the 4 units as a result of the pulses supplied.

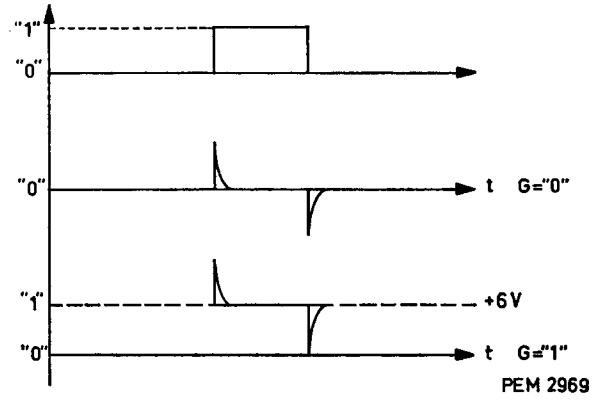


Fig. 4a

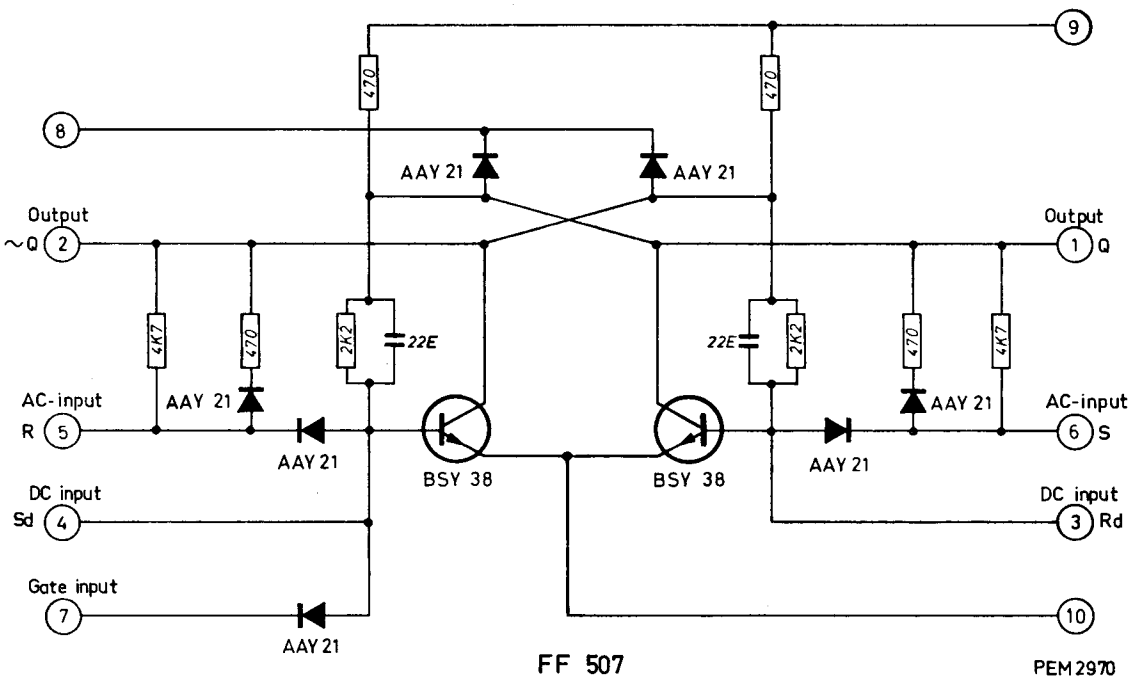


Fig. 5a

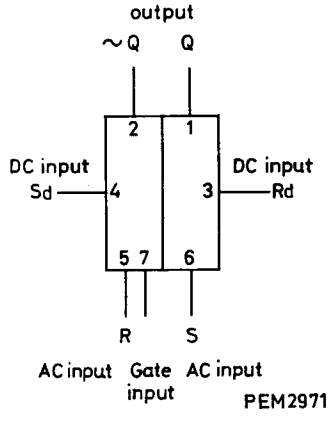


Fig. 5b

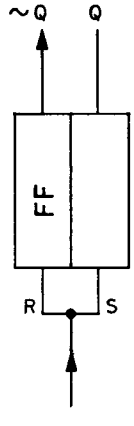


Fig. 6

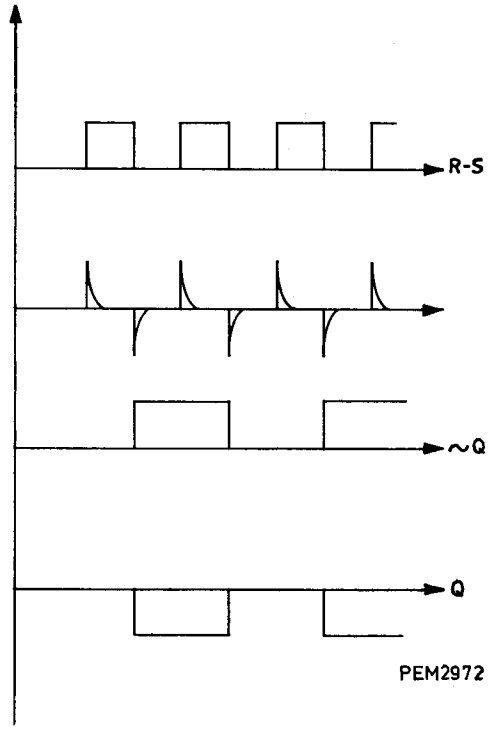


Fig. 7

	Flip-flop nr.							
	1		2		3		4	
Pulse nr.	∼Q1	Q1	∼Q2	Q2	∼Q3	Q3	∼Q4	Q4
	1	0	1	0	1	0	1	0
1	0	1	1	0	1	0	1	0
2	1	0	0	1	1	0	1	0
3	0	1	0	1	1	0	1	0
4	1	0	1	0	0	1	1	0
5	0	1	1	0	0	1	1	0
6	1	0	0	1	0	1	1	0
7	0	1	0	1	0	1	1	0
8	1	0	1	0	1	0	0	1
9	0	1	1	0	1	0	0	1
10	1	0	0	1	1	0	0	1
11	0	1	0	1	1	0	0	1
12	1	0	1	0	0	1	0	1
13	0	1	1	0	0	1	0	1
14	1	0	0	1	0	1	0	1
15	0	1	0	1	0	1	0	1
16	1	0	1	0	1	0	1	0

It may be seen that FF's no. 2, 3 and 4 only change position when the Q level of the proceding FF changes from "1" to "0" and not when it changes from "0" to "1".
A negative going step function will trigger the FF's, a positive one (from "0" to "1") gives a positive pulse which has no effect.

B. Pre-selecting counter

If the outputs ∼ Q, Q of the FF's in fig. 8 are used to control and AND gate for high, the signal at the gate-output will only be "1" after a certain number of pulses applied. If, for example, a signal from the AND gate is desired at the 11th pulse, it may be seen from the table that after this pulse the counter will have the following combinations (01, 01, 10, 01). The signal at Q of the first, the second, and the fourth FF will be "1", while the signal at ∼ Q of the third FF will be "1". If these signals of the FF's are connected to the AND-gate as shown in Fig. 9, only the signal "1" will be delivered by this gate during the time between the 11th and the 12th pulse, while at all other pulses the gate output will be "0".

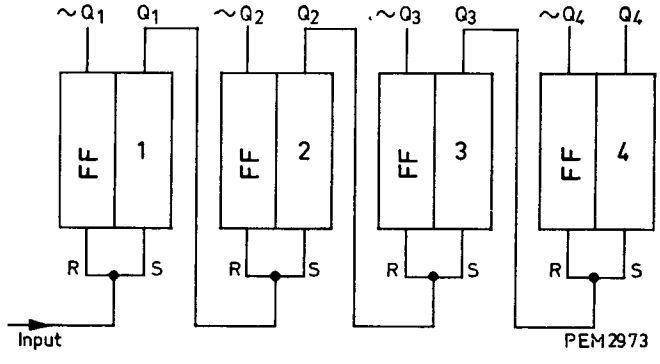


Fig. 8

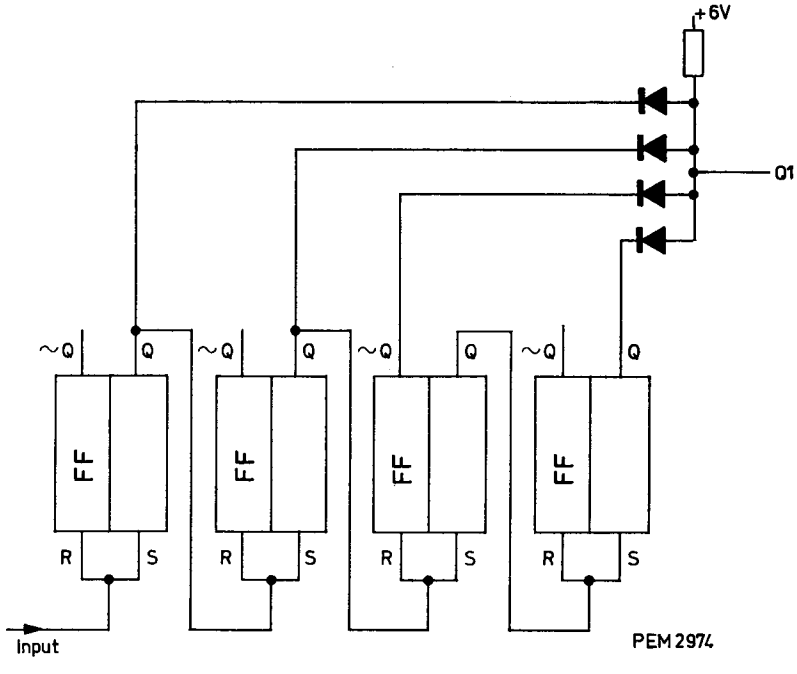


Fig. 9

C. Forward- and backward counting

When after a certain number of pulses the inputs (R-S) are connected to the $\sim$ Q terminals instead of the Q terminals (Fig. 10), the counting direction is inversed. It is assumed, for example, that twelve pulses have been counted, so that the combination will be (10, 10, 01, 01). Then the switch is changed over from Q to $\sim$ Q. When the next pulse is applied, $\sim$ Q of the first FF changes from "1" to "0" i.e. a negative pulse is delivered which triggers the next FF.

At terminals $\sim$ Q of the latter a negative going step function appears, too, which triggers the third FF. At terminal $\sim$ Q of this FF, however, a positive pulse appears. As this positive pulse does not trigger the succeeding FF, nothing more happens. Consequently, after the 13th pulse the combination will be (01, 01, 10, 01), which by means of the table is interpreted as 11. The counter counts forwards in the table-values, when the inputs (R-S) are connected to Q of the preceding FF while the counter counts down when connected to the $\sim$ Q terminals.

Of course in practice the change-over is not effected by means of mechanical switches, but is controlled by means of pulses, blocking either the $\sim$ Q or the Q output.

These pulses should not be too sharp, or else they might trigger the FF's. The control is effected as shown in Fig. 11. Here the gate GR1-R1 has been opened by means of a positive level, while the gate GR2-R2 has been closed by a negative level.

In case of counting down the level "phase" is changed, so that the Q output is closed, while the $\sim$ Q output is opened.

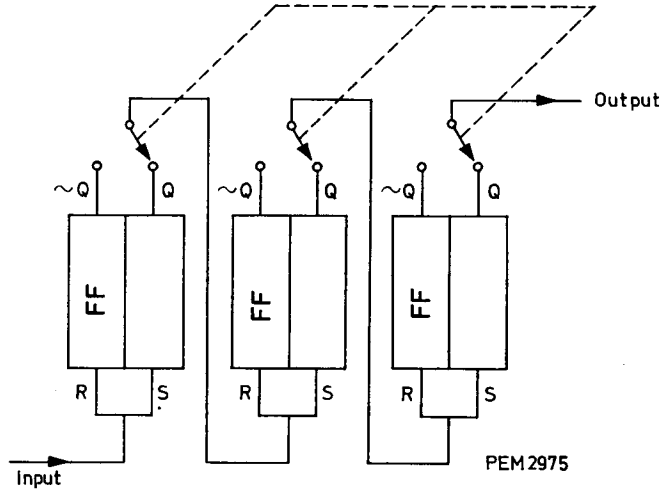


Fig. 10

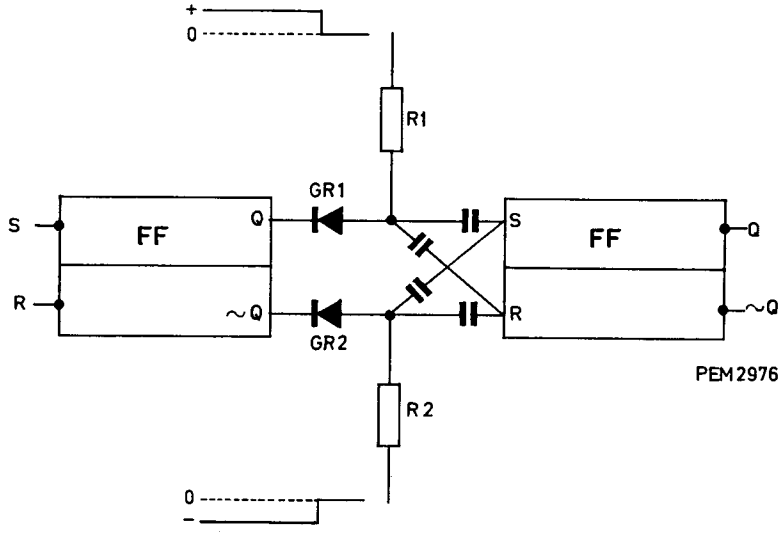


Fig. 11

D. Pre-setting of the counter

It is also possible to directly pre-set the counter to a certain figure, and then let it count down to 0.

It is assumed that the counter in Fig. 12 has been reset (position 0) and that the position of the FF's consequently is 10, 10, 10, 10.

If during counting, from the 4th pulse until the 12th pulse a negative rectangular pulse at the Q output of the last FF is desired, the counter is first pre-set to 11, equivalent to 01, 01, 10, 01. This setting is effected by actuating the individual FF's through the d.c. input (Rd) with appropiate pulses. In this case FF number 1, 2 and 4 are the ones to be actuated. After this the counter is set to backward counting, the pulses being taken from the $\sim$Q outputs, and with the 4th pulse the desired negative step function at the Q output of the last FF appears, and continues untill the 12th pulse. If desired all of the FF's can be reset (10, 10, 10, 10) by applying a negative pulse to input 7.

IV. Magnetic core memories

A. The magnetic core

The magnetic cores have a (nearly) rectangular hysteresis loop as shown in Fig. 13. If a magnetizing force +Hm is applied to the core, a flux density +Bm is produced in it. The value of Bm depends on the magnetic properties of the material.

When the magnetizing force is reduced to 0, the core still has a remanence of +B1. A magnetizing force of the opposite sign (–Hm) causes the flux to change sign too, so that the flux density changes from +B1 to –Bm.

If the magnetizing force is again removed, the flux density now changes from –Bm to –B1.

Thus in the absence of a magnetizing force the value of the flux density in the core will always be either +B1 or –B1, provided the same hysteresis loop is traversed.

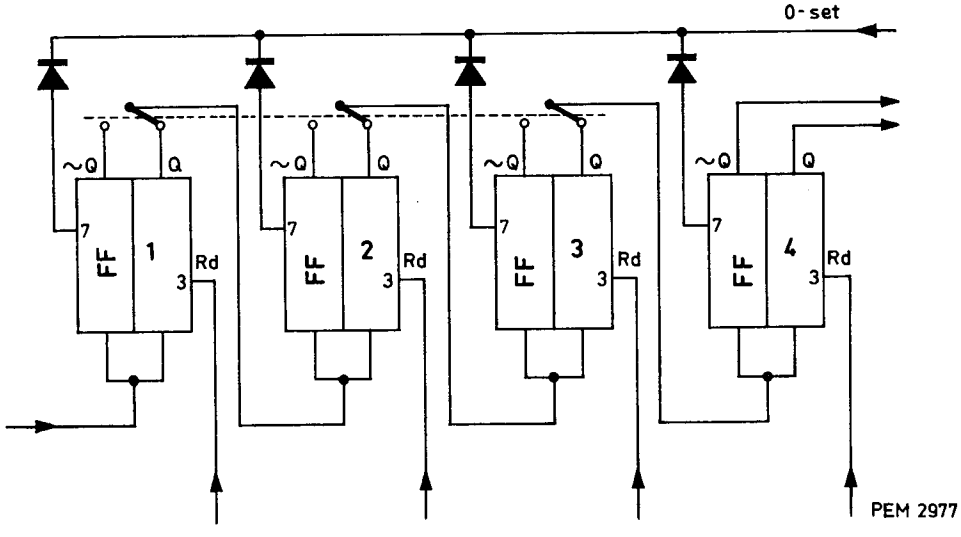
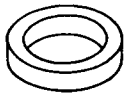


Fig. 12



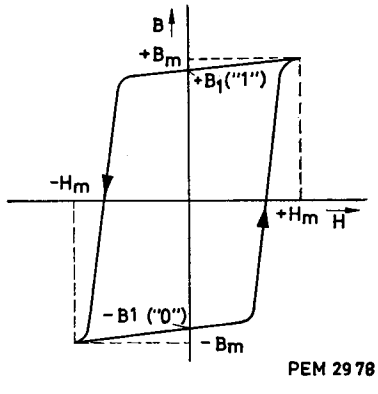


Fig. 13

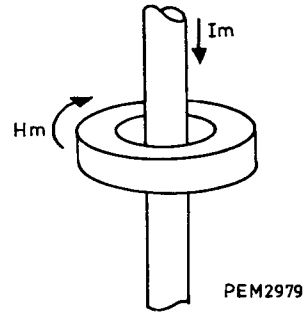


Fig. 14

The magnetic core has thus two stable states as far as the flux density is concerned, and can therefore be used to store one binary digit. The values "1" and "0" are assigned to the states +B1 and –B1 respectively. The core has the advantage over the flip-flop as a binary unit that it consumes no power in its stable states; it has the consequent disadvantage, however, that it is a passive element which cannot deliver an output pulse by itself.

In order to change the core from the state +B1 to the state –B1 a current Im (in practice a current pulse of amplitude Im) is passed through a wire which is threaded through the core (see Fig. 14). The magnitude and sign of Im are chosen so as to give rise to a magnetizing force of –Hm. A current pulse of the same amplitude in the opposite direction causes the core to revert to its former state.

An e.m.f. is produced in the wire as a result of the reversal of state of the core. The magnitude of this e.m.f. is determined by the rate of change of flux: $-d\Phi / dt$. Advantage is taken of this property to determine the state of the core at a given time ("reading" or "sensing" the core).

A separate wire called the "read" wire which will be discussed further below is used for this purpose instead of the current carrying "write" wire.

B. Coincidence

In the ferrite core matrix the magnetizing forces needed to change the state of a given core are produced by two currents in two separate wires, both of which are threaded through the core (see Fig. 15). The current in each wire has the value ½ Im, so that the combined effect of the two currents will be enough to change the state of the core, but one current alone will have no effect on the flux density thanks to the rectangular form of the hysteresis loop. This may be seen from Fig. 16.

When the core is in the state of negative remanence –B1 (the "0" state), a positive pulse of magnitude ½ Im will cause it to trace the hysteresis loop from –B1 to "a" and back again. A pulse of twice this amplitude (+Im) on the other hand will change the state irreversibly for –B1 to +B1 (the "-" state) via "a" and "b". A similar effect will be produced with negative current pulses when the core is in the "1" state (+B1). When the core is in the "0" state a negative current pulse (–½ Im or –Im) will have practically no effect on the flux density, and similarly a positive pulse (+½ Im or +Im) will leave the state of a core unchanged if it is originally in the "1" state.

The information given above is summarized in the following tabel:

original state of core	current pulse	resultant state of core	change of state
0	+ Im	1	yes
0	+½ Im	0	no
0	–½ Im	0	no
0	– Im	0	no
1	+ Im	1	no
1	+½ Im	1	no
1	–½ Im	1	no
1	– Im	0	yes

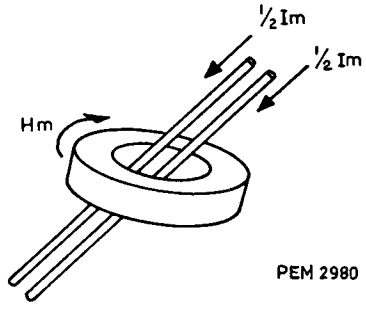


Fig. 15

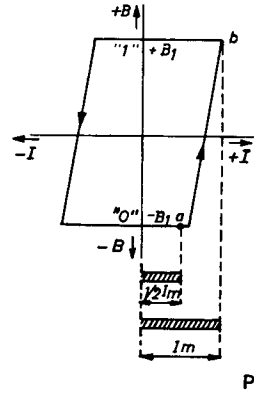


Fig. 16

C. Reading or sensing the core

A third wire, the read wire, is threaded through the matrix. This wire is marked R in Fig. 17. The voltage pulses induced in the read wire are used as an indication of the change of state of a core.

D. Deviations from ideality

Although a current pulse $+\frac{1}{2}$ Im or $-\frac{1}{2}$ Im does not change the state of the core, it does in fact cause a slight permanent change in the value of the flux density, because the hysteresis loop is not perfectly rectangular. This is shown in Fig. 18, where the consequences of applying such a current pulse to the core in state "0" are shown.

As the current falls off from its maximum value, the flux density follows a smaller hysteresis loop, returning to a value –B1′, which is smaller than –B1. This state is called the "disturbed 0" state.

When a pulse +Im is applied to this core so as to change it from –B1′ to +B1, the change in flux density will be smaller than in the case of the initial flux density being –B1. Thus a half current pulse will excite a small pulse in the read wire, while a change of state in a disturbed core will give rise to an e.m.f. in the read wire which is smaller than the ideal. In order that these disturbed read pulses can be distinguished from the required read pulses in unfavourable cases, special measures must be taken.

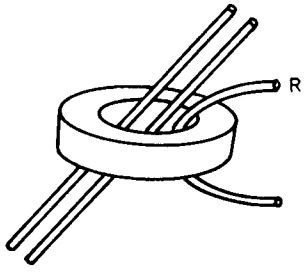


Fig. 17

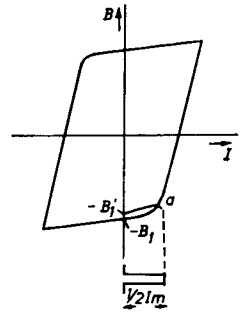


Fig. 18

XXVI Access to and replacement of parts

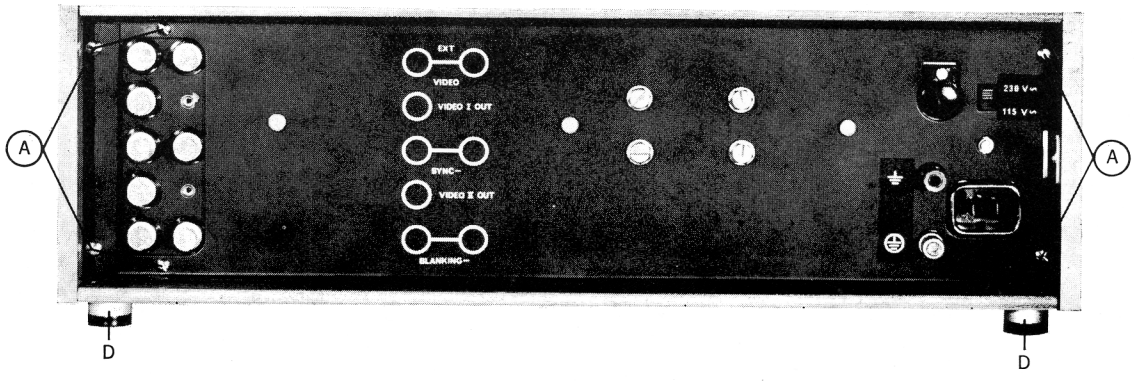


Fig. XXVI-1 Rear view

A. Removing the cabinet panels

The cabinet consists of a number of panels which can be removed separately.

1. Rear panel
a. Loosen the 6 screws "A" (see Fig. XXVI-1)
b. Remove the rear plate.

2. Top panel
a. Pull the springs at the rear corners of the panel, while lifting the rear of the panel
b. Push the panel forward and remove it.

3. Bottom panel
a. Place the instrument upside down
b. Remove the 4 feet "D" (see Fig. XXVI-1)
c. Pull the springs at the rear corners of the panel, while lifting the rear of the panel
d. Push the panel forward and remove it.

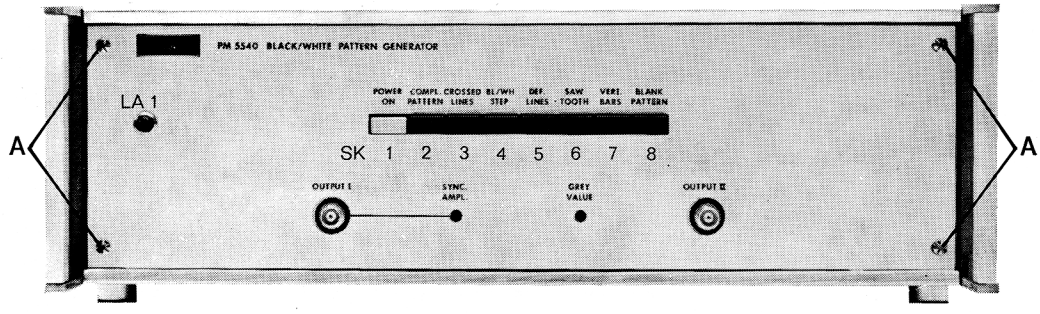


Fig. XXVI-2 Front view

B. Removing the front panel

a. Loosen the 4 screws "A" (see Fig. XXVI-2)
b. Pull the plate, placed on a slide, forward and turn it down.
   The front panel components are now accessible.

XXVII Maintenance

A. Switches

Should the switches cease function properly due to rity contacts, they should be treated with switch oil (see list of mechanical parts).
This oil has both cleaning and lubricating properties.
After using this oil, the switch should be operated a few times.

B. Cabinet panels

The P.V.C. coated cabinet panels, can be cleaned with soap and water (first remove the panel from the casing, chapter XXVI). If necessary, a fine scouring detergent can be used.

XXVIII List of mechanical parts

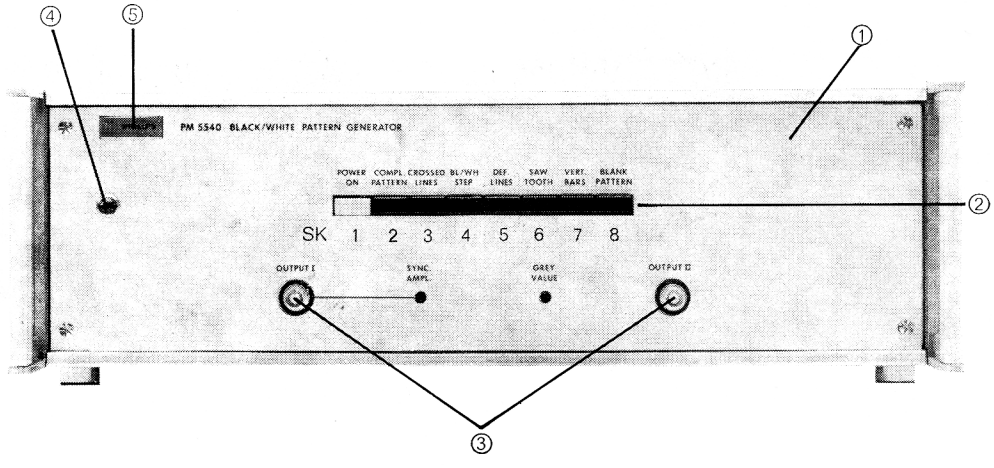


Fig. XXVIII-1 Front view of the instrument

Item	Description	Quantity	Ordering number
1	Text plate	1	4822 455 70048
2	Push-button unit	1	4822 276 80026
3	BNC-connector	2	4822 267 10004
4	Lamp-holder	1	4822 255 10025
5	Badge	1	4822 459 10086

6	BNC-connector	8	4822 267 10004
7	Earth connector	1	4822 290 40012
8	Earth connector	1	4822 290 40011
9	Socket (mains. con.) (2 pole)	1	4822 265 20027
9	Socket (mains. con.) (3 pole)	1	4822 265 30066
10	Switch	1	4822 277 20014

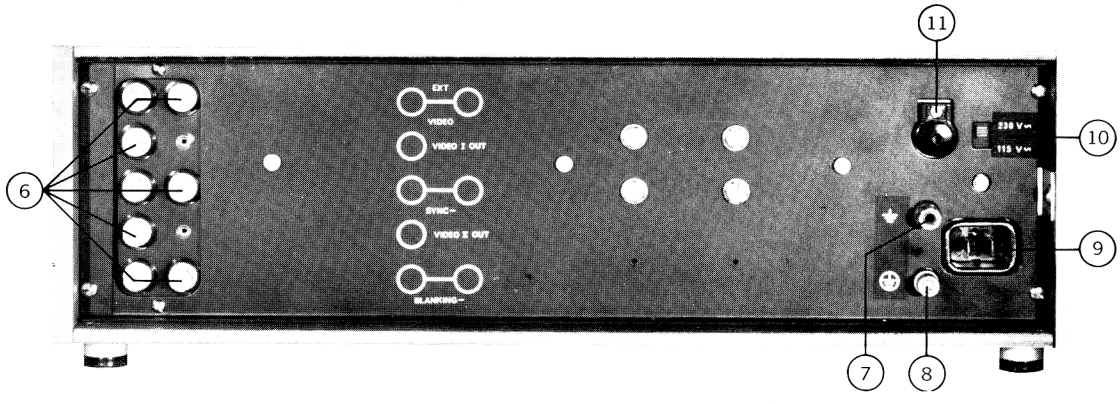


Fig. XXVIII-2 Rear view of the instrument

11	Fuse holder	1	4822 256 40012
	Contact block	18	4822 267 70043
	BNC-connector (cable-part)		4822 265 10003
	Terminating plug 75 Ω		4822 264 10024
	Coaxial cable 75 Ω		4822 320 10028
	Mains flex		4822 321 10071
	Fuse for 230 V operation		4822 253 30013
	Fuse for 115 V operation		4822 253 30017
	10 cc of switch oil		4822 390 10007

XXIX List of electrical parts

This parts list does not contain multi-purpose and standard parts. These components are indicated in the circuit diagram by means of identification marks. The specification can be derived from the survey below.

Diese Ersatzteilliste enthält keine Universal- und Standard-Teile. Diese sind im jeweiligen Prinzipschaltbild mit Kennzeichnungen versehen. Die Spezifikation kann aus nachstehender Übersicht abgeleitet werden.

In deze stuklijst zijn geen universele en standaardonderdelen opgenomen. Deze componenten zijn in het principeschema met een merkteken aangegeven. De specificatie van deze merktekens is hieronder vermeld.

La présente liste ne contient pas des pièces universelles et standard. Celles-ci ont été repérées dans le schéma de principe. Leurs specifications sont indiquées ci-dessous.

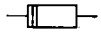
Esta lista de componentes no comprende componentes universales ni standard. Estos componentes están provistos en el esquema de principio de una marca. El significado de estas marcas se indica a continuación.

Carbon resistor E24 series
Kohleschichtwiderstand, Reihe E24
Koolweerstand E24 reeks
Résistance au carbone, série E24
Resistencia de carbón, serie E24
0,125 W 5%

Carbon resistor E12 series
Kohleschichtwiderstand, Reihe E12
Koolweerstand E12 reeks
Résistance au carbone, série E12
Resistencia de carbón, serie E12
0,25 W ≦ 1 MΩ, 5%
> 1 MΩ, 10%

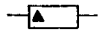
Carbon resistor E24 series
Kohleschichtwiderstand, Reihe E24
Koolweerstand E24 reeks
Résistance au carbone, série E24
Resistencia de carbón, serie E24
0,5 W ≦ 5 MΩ, 1%
> 5 ≦ 10 MΩ, 2%
> 10 MΩ, 5%

Carbon resistor E12 series
Kohleschichtwiderstand, Reihe E12
Koolweerstand E12 reeks
Résistance au carbone, série E12
Resistencia de carbón, serie E12
0,5 W ≦ 1,5MΩ, 5%
> 1,5MΩ, 10%

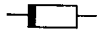


Wire-wound resistor
Drahtwiderstand
Draadgewonden weerstand
Résistance bobinée
Resistencia bobinada
10 W 5%

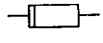
Carbon resistor E12 series
Kohleschichtwiderstand, Reihe E12
Koolweerstand E12 reeks
Résistance au carbone, série E12
Resistencia de carbón, serie E12
1 W ≦ 2,2 MΩ, 5%
> 2,2 MΩ, 10%



Carbon resistor E12 series
Kohleschichtwiderstand, Reihe E12
Koolweerstand E12 reeks
Résistance au carbone, série E12
Resistencia de carbón, serie E12
2 W 5%



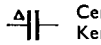
Wire-wound resistor
Drahtwiderstand
Draadgewonden weerstand
Résistance bobinée
Resistencia bobinada
0,4 – 1,8 W 0,5%



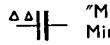
Wire-wound resistor
Drahtwiderstand
Draadgewonden weerstand
Résistance bobinée
Resistencia bobinada
5,5 W ≦ 200 Ω, 10%
> 200 Ω, 5%

Tubular ceramic capacitor
Rohrkondensator
Keramische kondensator, buistype
Condensateur céramique tubulaire
Condensador cerámico tubular
500 V

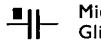
Tubular ceramic capacitor
Rohrkondensator
Keramische kondensator, buistype
Condensateur céramique tubulaire
Condensador cerámico tubular
700 V



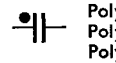
Ceramic capacitor, "pin-up"
Keramikkondensator "Pin-up" (Perltyp)
Keramische kondensator "Pin-up" type
Condensateur céramique, type perle
Condensador cerámico, versión "colgable"
500 V



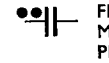
"Microplate" ceramic capacitor
Miniatur-Scheibenkondensator
"Microplate" keramische kondensator
Condensateur céramique "microplate"
Condensador cerámico "microplaca"
30 V



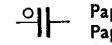
Mica capacitor
Glimmerkondensator
Micakondensator
Condensateur au mica
Condensador de mica
500 V



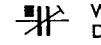
Polyester capacitor
Polyesterkondensator
Polyesterkondensator
Condensateur au polyester
Condensador polyester
400 V



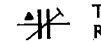
Flat-foil polyester capacitor
Miniatur-Polyesterkondensator (flach)
Platte miniatuur polyesterkondensator
Condensateur au polyester, type plat
Condensador polyester, tipo de placas planas
250 V



Paper capacitor
Papierkondensator
Papierkondensator
Condensateur au papier
Condensador de papel
1000 V



Wire-wound trimmer
Drahttrimmer
Draadgewonden trimmer
Trimmer à fil
Trimmer bobinado



Tubular ceramic trimmer
Rohrtrimmer
Buisvormige keramische trimmer
Trimmer céramique tubulaire
Trimmer cerámico tubular

For multi-purpose and standard parts, please see PHILIPS' Service Catalogue.
Für die Universal- und Standard-Teile siehe den PHILIPS Service-Katalog.
Voor universele en standaardonderdelen raadplege men de PHILIPS Service Catalogus.
Pour les pièces universelles et standard veuillez consulter le Catalogue Service PHILIPS.
Para piezas universales y standard consulte el Catálogo de Servicio PHILIPS.

Print Panels

Unit	Description	Print number	Ordering number
1	Power supply	4008 108 76520	4822 212 70135
2	Ext. board	4008 108 70020	4822 263 70011
3	Register A2	4008 108 70030	4822 212 70029
4	Register A1	4008 108 70040	4822 212 70031
5	Memory E version	4008 108 70050	4822 212 70032
5	Memory A version	4008 108 71540	4822 212 70134
6	Line decoder*	4008 108 70060	4822 212 70033
7	Line register*	4008 108 70070	4822 212 70034
8	Interval decoder	4008 108 70080	4822 212 70035
9	Hor. decoder	4008 108 70090	4822 212 70036
10	Hor. divider	4008 108 70100	4822 212 70037
11	Vert. decoder	4008 108 70110	4822 212 70038
12	Vert. divider*	4008 108 74140	4822 212 70137
13	Black/white steps	4008 108 70130	4822 212 70041
14	Linear gate	4008 108 70140	4822 212 70042
15	Cross-bar gate	4008 108 70150	4822 212 70043
16	Output	4008 108 70160	4822 212 70044
17	Input	4008 108 74130	4822 212 70136
18	Connection board	4008 108 74110	4822 466 10171

*) After modification, these units can also be used for the PM5540A (RTMA-version).
Modifications are reflected in the circuit diagrams (see also printed wiring-boards of the A version).

Diagram number	Description	Value	Watt/Volt	Ordering number
Unit 1				
C1	electrolytic capacitor	160 µF	40 V	4822 124 20396
C2	electrolytic capacitor	64 µF	16 V	4822 124 20089
C3	electrolytic capacitor	100 µF	10 V	4822 124 20384
C4-C5	electrolytic capacitor	160 µF	4 V	4822 124 20053
C6	electrolytic capacitor	1600 µF	40 V	4822 124 40003
C7-C8	electrolytic capacitor	2500 µF	25 V	4822 124 30009
GR2-GR4		B30/C600		4822 130 50183
GR3		B30/C1600		4822 130 50185
R11-R14	resistor	2.2 Ω	1 %	4822 113 60078
T1	transformer			4822 146 40102
Unit 3				
CB1 . . . CB6	circuit block	FF507		4822 209 80001
C30-C31	electrolytic capacitor	100 µF	10 V	4822 124 20384
Unit 4				
CB1 . . . CB6	circuit block	FF507		4822 209 80001
C28-C29	electrolytic capacitor	100 µF	10 V	4822 124 20384
C30	electrolytic capacitor	64 µF	16 V	4822 124 20089
Unit 5				
C2	capacitor	470 kpF	250 V	4822 121 40015
C3	electrolytic capacitor	32 µF	16 V	4822 124 20097
C4	electrolytic capacitor	100 µF	10 V	4822 124 20384
R24-R26	resistor	39 Ω	1 W	4822 112 20069
T1 . . . T8	transformer			4822 142 60081
Unit 6				
C2-C3	electrolytic capacitor	100 µF	10 V	4822 124 20384
L1-L2	coil			4822 158 10038
Unit 7				
CB1 . . . CB5	circuit block	FF507		4822 209 80001
C22-C24	electrolytic capacitor	100 µF	10 V	4822 124 20384
L1-L2	coil			4822 158 10038
Unit 8				
C1-C2	capacitor	22 pF	500 V	4822 120 10063
C3-C4	electrolytic capacitor	100 µF	10 V	4822 124 20384
L1	coil			4822 158 10038
Unit 9				
CB1 . . . CB3	circuit block	FF507		4822 209 80001
C15-C16	electrolytic capacitor	100 µF	10 V	4822 124 20384
L1-L2	coil			4822 158 10038

Diagram number	Description	Value	Watt/Volt	Ordering number
Unit 10				
CB1 . . . CB6	circuit block	FF507		4822 209 80001
C2	capacitor	1000 pF	250 V	4822 121 40029
C3	capacitor	22 kpF	400 V	4822 120 40143
C19	electrolytic capacitor	100 µF	10 V	4822 124 20384
C20	electrolytic capacitor	50 µF	10 V	4822 124 20373
C21	electrolytic capacitor	32 µF	10 V	4822 124 20097
R2-R3	resistor	1 kΩ	0.125 W	4822 116 50274
L1 . . . L3	coil			4822 158 10038
Unit 11				
CB1 . . . CB7	circuit block	FF507		4822 209 80001
C16-C17	electrolytic capacitor	100 µF	10 V	4822 124 20384
L1-L2	coil			4822 158 10038
Unit 12				
CB1 . . . CB6	circuit block	FF507	10 V	4822 209 80001
C15-C16	electrolytic capacitor	100 µF	10 V	4822 124 20384
L1-L2	coil			4822 158 10038
Unit 14				
C12-C13	electrolytic capacitor	100 µF	10 V	4822 124 20384
C14	electrolytic capacitor	64 µF	16 V	4822 124 20089
R47-R48	resistor	1 kΩ	1 %	4822 116 50274
R53-R54	resistor	4.7 kΩ	1 %	4822 116 50117
L1 . . . L3	coil			4822 158 10038
Unit 15				
CB1	circuit block	FF507		4822 209 80001
C9-C10	capacitor	330 kpF	250 V	4822 121 40009
C11	capacitor	470 kpF	250 V	4822 121 40015
C14-C15	electrolytic capacitor	100 µF	10 V	4822 124 20384
L1 . . . L4	coil			4822 158 10038
Unit 16				
C1	electrolytic capacitor	16 µF	10 V	4822 124 20357
C3	electrolytic capacitor	32 µF	16 V	4822 124 20097
C5-C7	electrolytic capacitor	320 µF	10 V	4822 124 20402
C6-C8	electrolytic capacitor	64 µF	10 V	4822 124 20089
C10	capacitor	100 kpF	400 V	4822 121 40012
C11	electrolytic capacitor	50 µF	10 V	4822 124 20374
C12 . . . C15	electrolytic capacitor	100 µF	10 V	4822 124 20384
C16 . . . C18	electrolytic capacitor	64 µF	10 V	4822 124 20089
R8	potentiometer	500 Ω		4822 100 10038
R24-R40	potentiometer	5 kΩ		4822 100 10079
L1 . . . L7	coil			4822 158 10038

Diagram number	Description	Value	Watt-/Volt	Ordering number
Unit 17				
CB1-CB2	circuit block	FF507		4822 209 80001
C1-C6	capacitor	1 μF	100 V	4822 121 40176
C2-C7	capacitor	100 kpF	100 V	4822 121 40036
C3-C4-C8-C9	electrolytic capacitor	10 μF	16 V	4822 124 20353
C11	capacitor	150 pF	100 V	4822 121 50416
C14	capacitor	15 kpF	63 V	4822 121 50279
C15-C18	capacitor	1 kpF	500 V	4822 121 50186
C20	capacitor	100 pF	160 V	4822 121 50411
C21	capacitor	3.3 kpF	125 V	4822 121 50235
C24	capacitor	820 pF	250 V	4822 120 60105
C26-C27	electrolytic capacitor	100 μF	10 V	4822 124 20384
C28	electrolytic capacitor	16 μF	10 V	4822 124 20357
C29	electrolytic capacitor	64 μF	16 V	4822 124 20089
R26	resistor	47 kΩ	0.125 W	4822 116 50108
R27	potentiometer	50 kΩ		4822 100 10079
R50	potentiometer	5 kΩ		4822 100 10036
L1 . . . L3	coil			4822 158 10038

Transistors

Type number	Ordering number
ASY27	4822 130 40269
ASY29	4822 130 40092
ASZ16	4822 130 40279
ASZ21	4822 130 40271
BCY32	4822 130 40289
BCY40	4822 130 40372
BCY39	4822 130 40125
OC123	4822 130 40278
2N930	4822 130 40051
2N2362	4822 130 40467
2N2369	4822 130 40407
2N2894	4822 130 40018
2N2904	4822 130 40388
2N2905	4822 130 40021
AC188	4822 130 40456

Diodes

Type number	Ordering number
AAY11	4822 130 30269
AAY21	4822 130 30087
BAY32	4822 130 30303
BAY38	4822 130 30256
BAX16	4822 130 30273
BZY56	4822 130 30129
BZY59	4822 130 30132
BZY60	4822 130 30196
BZY63	4822 130 30245
BZY88/C5V6	4822 130 30193
AAZ15	4822 130 30229